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(54) **DISPLAY DEVICE AND METHOD FOR DRIVING SAME**

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CPC ***G09G 3/3283*** (2013.01); ***G09G 3/325*** (2013.01); *G09G 2330/028* (2013.01); *G09G 2300/0426* (2013.01); *G09G 2320/0633* (2013.01); *G09G 2320/046* (2013.01); *G09G 2300/0819* (2013.01); *G09G 2300/0842* (2013.01); *G09G 2320/0295* (2013.01)

(57) **ABSTRACT**

A display device that can compensate for degradation of circuit elements while suppressing an increase in circuit size is implemented.

A data signal line (S(j)) is not only used as a signal line that transfers a signal for allowing an organic EL element (OLED) in each pixel circuit (**11**) to emit light at a desired luminance, but also used as a signal line for characteristic detection. In addition, a switch (**334**) is provided between the data signal line (S(j)) and an internal data line (Sin(j)). In such a configuration, during an AD conversion period during which analog data obtained for characteristic detection is converted into digital data, the switch (**334**) is brought into an off state and a potential of the data signal line (S(j)) obtained immediately before the AD conversion period is supplied from through a predetermined control line (CL) to the data signal line (S(j)).

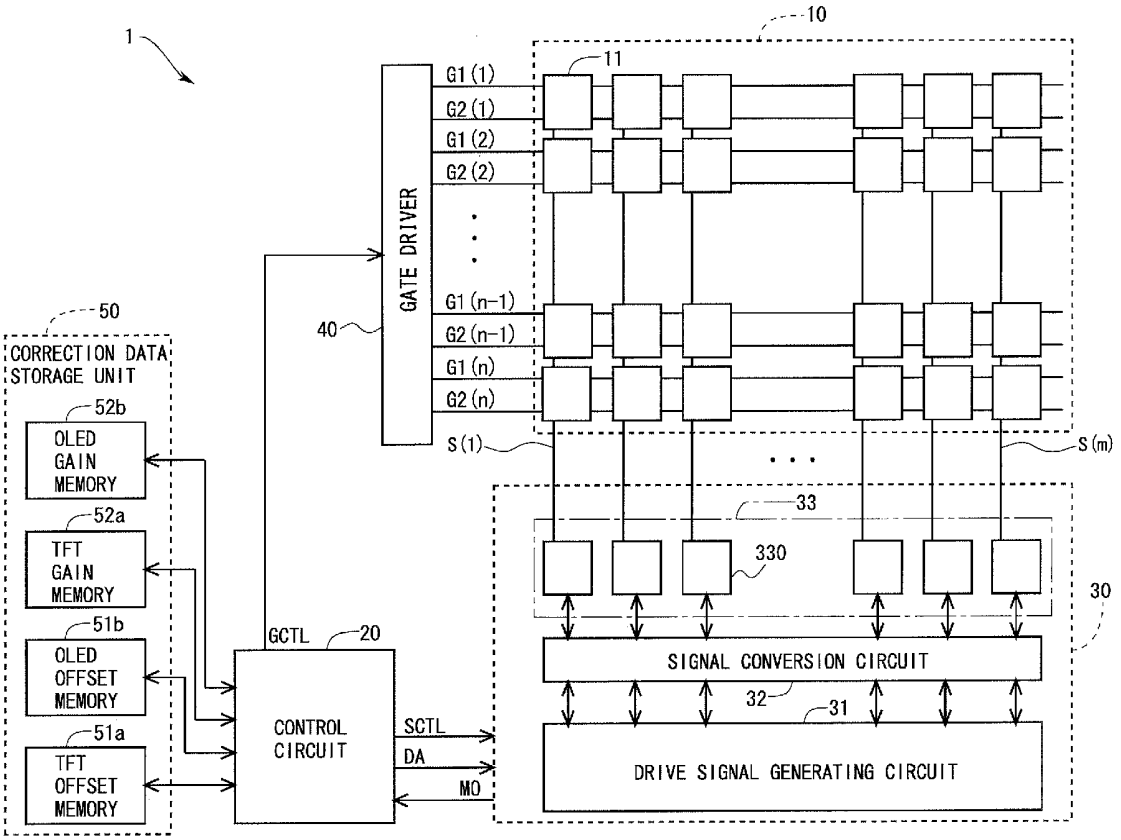


Fig.1

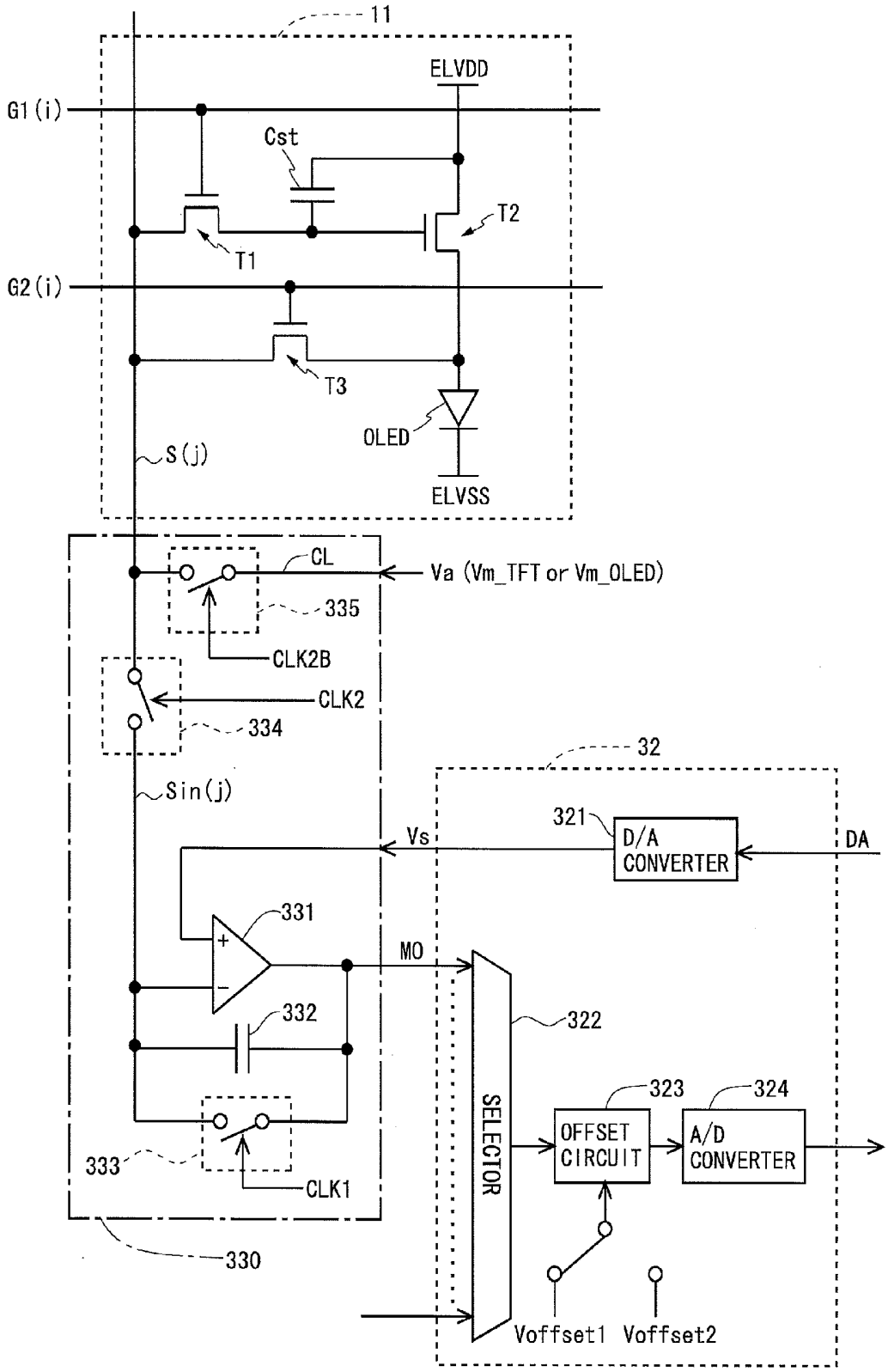

11
ELVDD
G1(i)
Cst
T2
T1
G2(i)
T3
OLED
S(j)
ELVSS
CL
Va (Vm_TFT or Vm_OLED)
335
CLK2B
CLK2
334
32
Sin(j)
321
D/A CONVERTER
Vs
DA
331
MO
332
322
SELECTOR
323
324
OFFSET CIRCUIT
A/D CONVERTER
333
CLK1
330
Voffset1
Voffset2

Fig.2

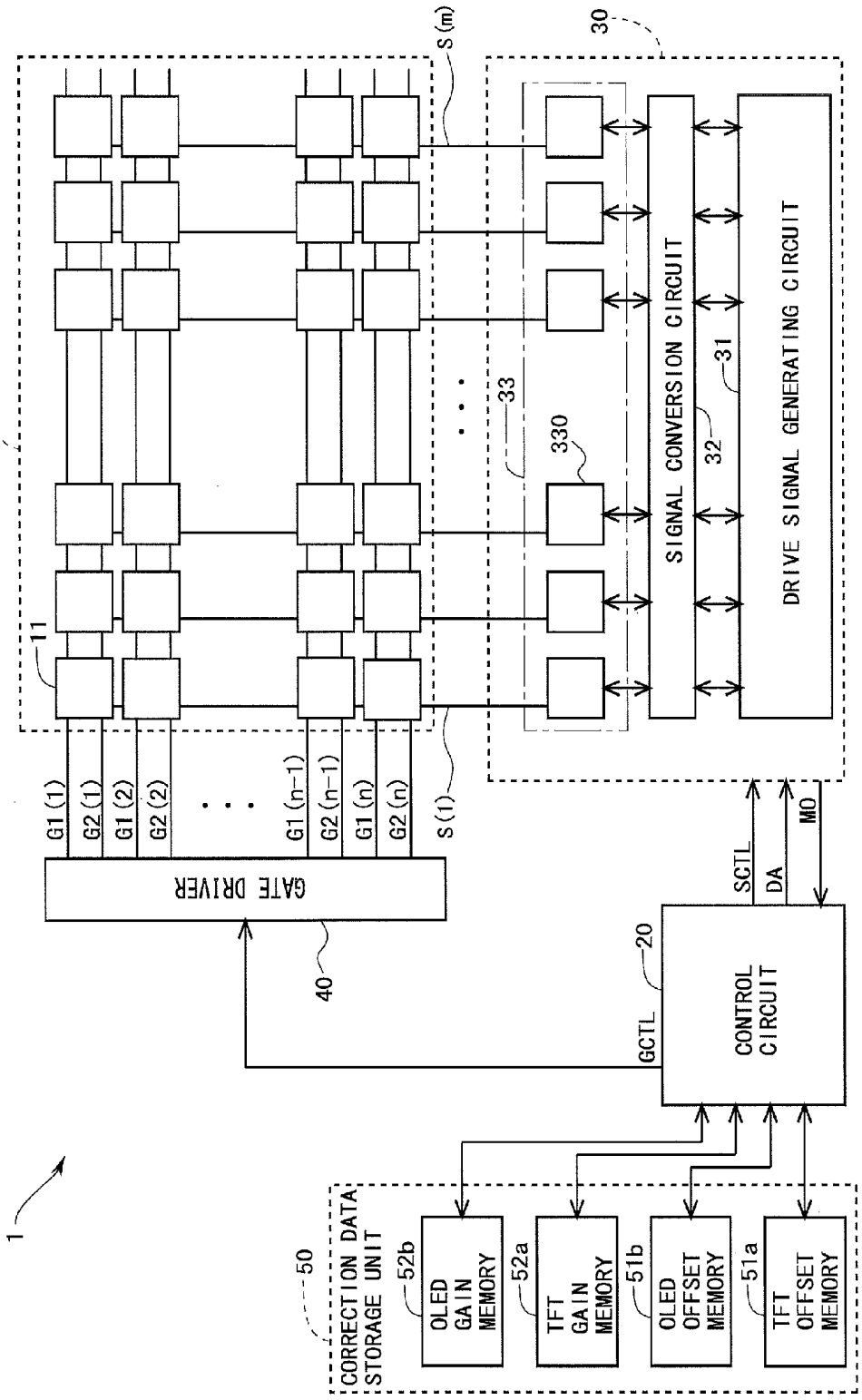

1
10
11
30
31
32
33
330
S(m)
S(1)
G1(1)
G2(1)
G1(2)
G2(2)
G1(n-1)
G2(n-1)
G1(n)
G2(n)
GATE DRIVER
40
SIGNAL CONVERSION CIRCUIT
DRIVE SIGNAL GENERATING CIRCUIT
SCTL
DA
MO
GCTL
20
CONTROL CIRCUIT
50
CORRECTION DATA STORAGE UNIT
52b
OLED GAIN MEMORY
52a
TFT GAIN MEMORY
51b
OLED OFFSET MEMORY
51a
TFT OFFSET MEMORY

Fig.3

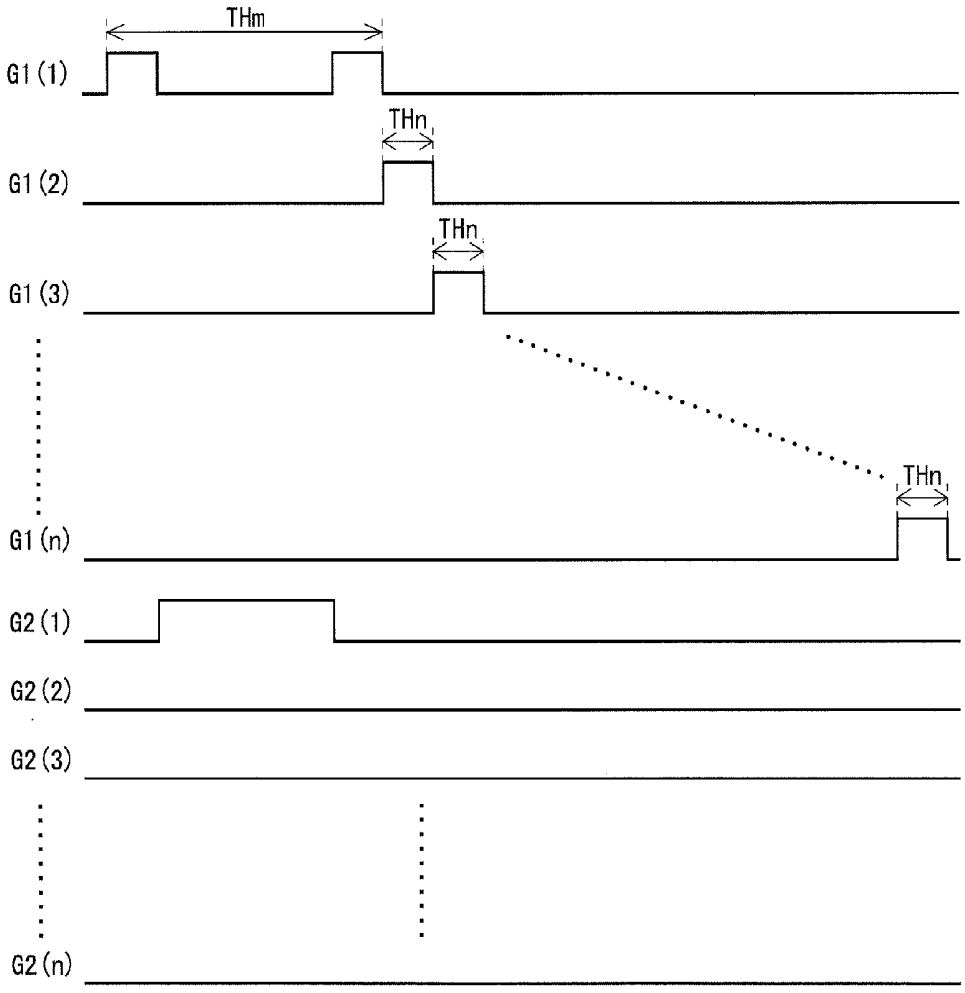


Fig.4

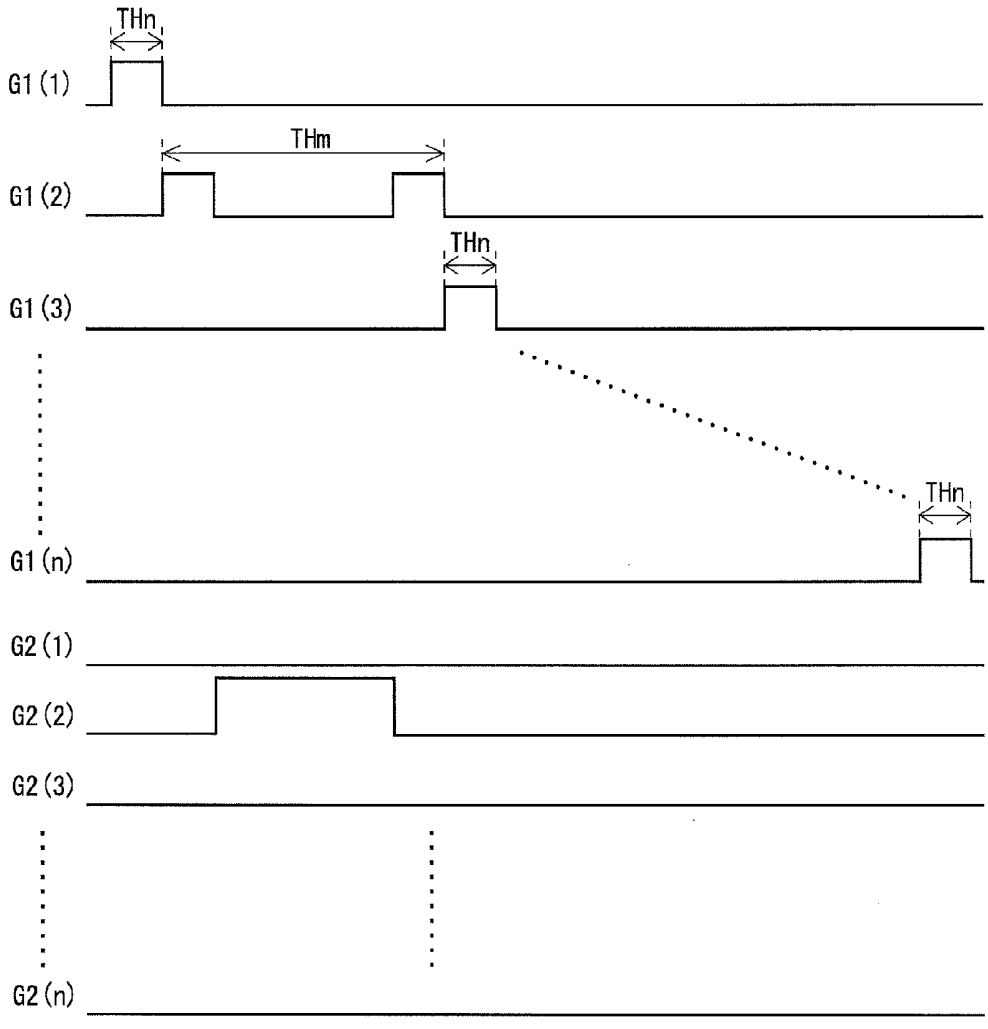


Fig.5

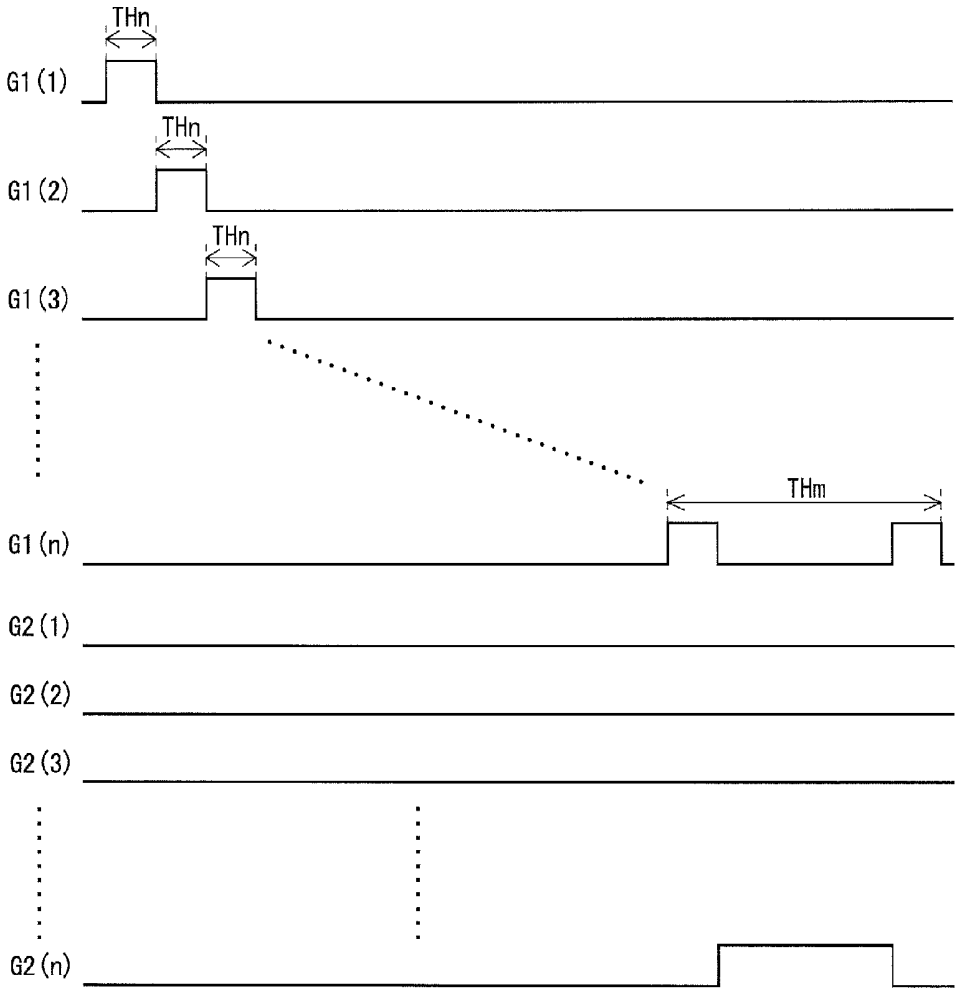


Fig.6

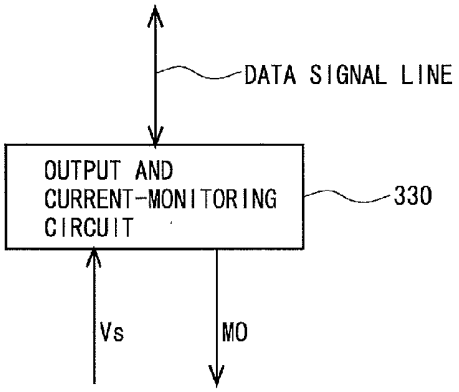

DATA SIGNAL LINE
OUTPUT AND
CURRENT-MONITORING
CIRCUIT
330
Vs
MO

Fig.7

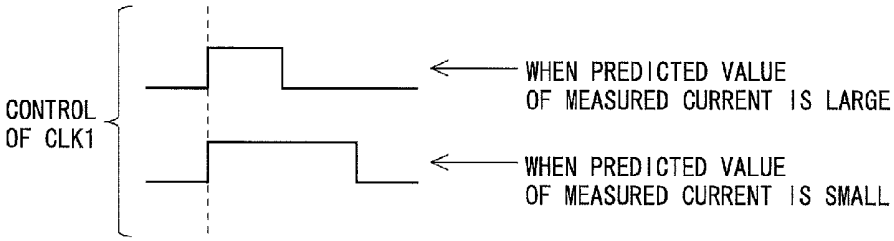

CONTROL
OF CLK1
WHEN PREDICTED VALUE
OF MEASURED CURRENT IS LARGE
WHEN PREDICTED VALUE
OF MEASURED CURRENT IS SMALL

Fig.8

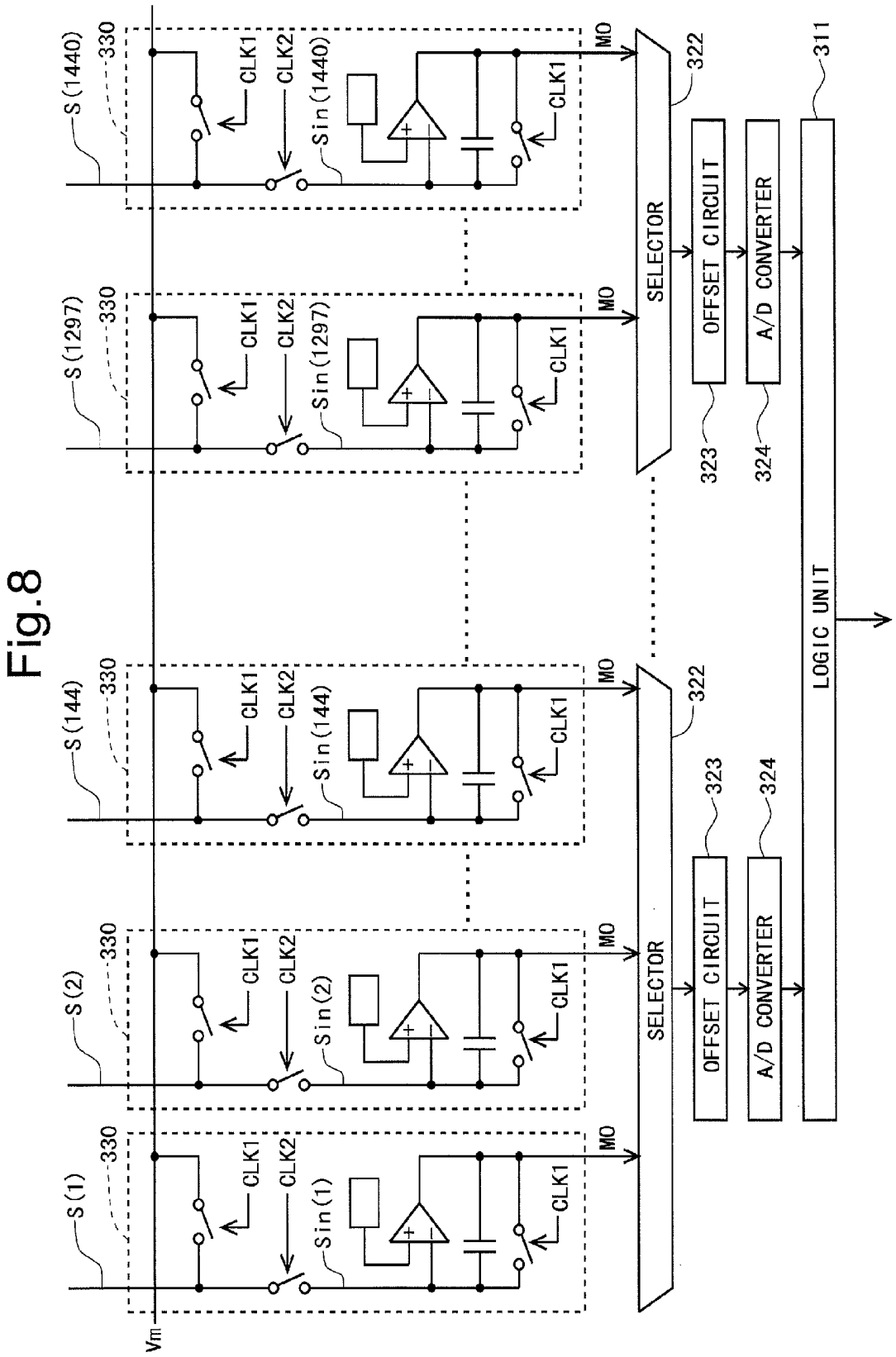

S(1440)
330
CLK1
CLK2
Sin(1440)
CLK1
MO
S(1297)
330
CLK1
CLK2
Sin(1297)
CLK1
MO
SELECTOR
322
OFFSET CIRCUIT
323
A/D CONVERTER
324
LOGIC UNIT
311
S(144)
330
CLK1
CLK2
Sin(144)
CLK1
MO
S(2)
330
CLK1
CLK2
Sin(2)
CLK1
MO
S(1)
330
CLK1
CLK2
Sin(1)
CLK1
MO
Vm

Fig.9

	CHARACTERISTIC DETECTION OPERATION	NORMAL OPERATION
(k+1)TH FRAME	FIRST ROW	SECOND TO nTH ROWS
(k+2)TH FRAME	SECOND ROW	FIRST ROW AND THIRD TO nTH ROWS
(k+3)TH FRAME	THIRD ROW	FIRST TO SECOND ROWS AND FOURTH TO nTH ROWS
.....	.....	.....
(k+n)TH FRAME	nTH ROWS	FIRST TO (n-1)TH ROW

Fig.10

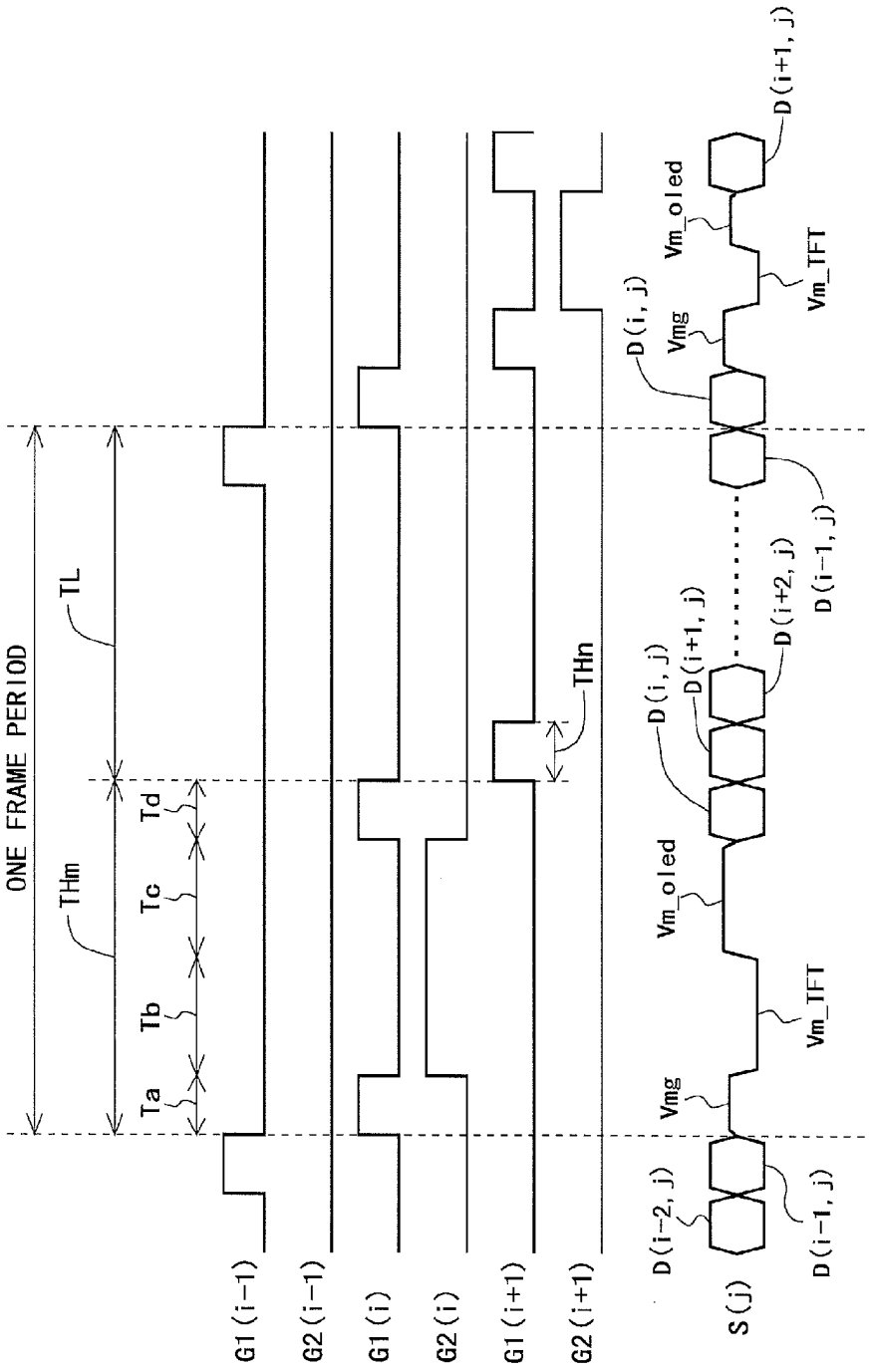

ONE FRAME PERIOD
TL
THm
Ta
Tb
Tc
Td
THn
G1 (i−1)
G2 (i−1)
G1 (i)
G2 (i)
G1 (i+1)
G2 (i+1)
S(j)
D(i−2, j)
D(i−1, j)
D(i, j)
D(i+1, j)
D(i+2, j)
Vmg
Vm_oled
Vm_TFT

Fig.11

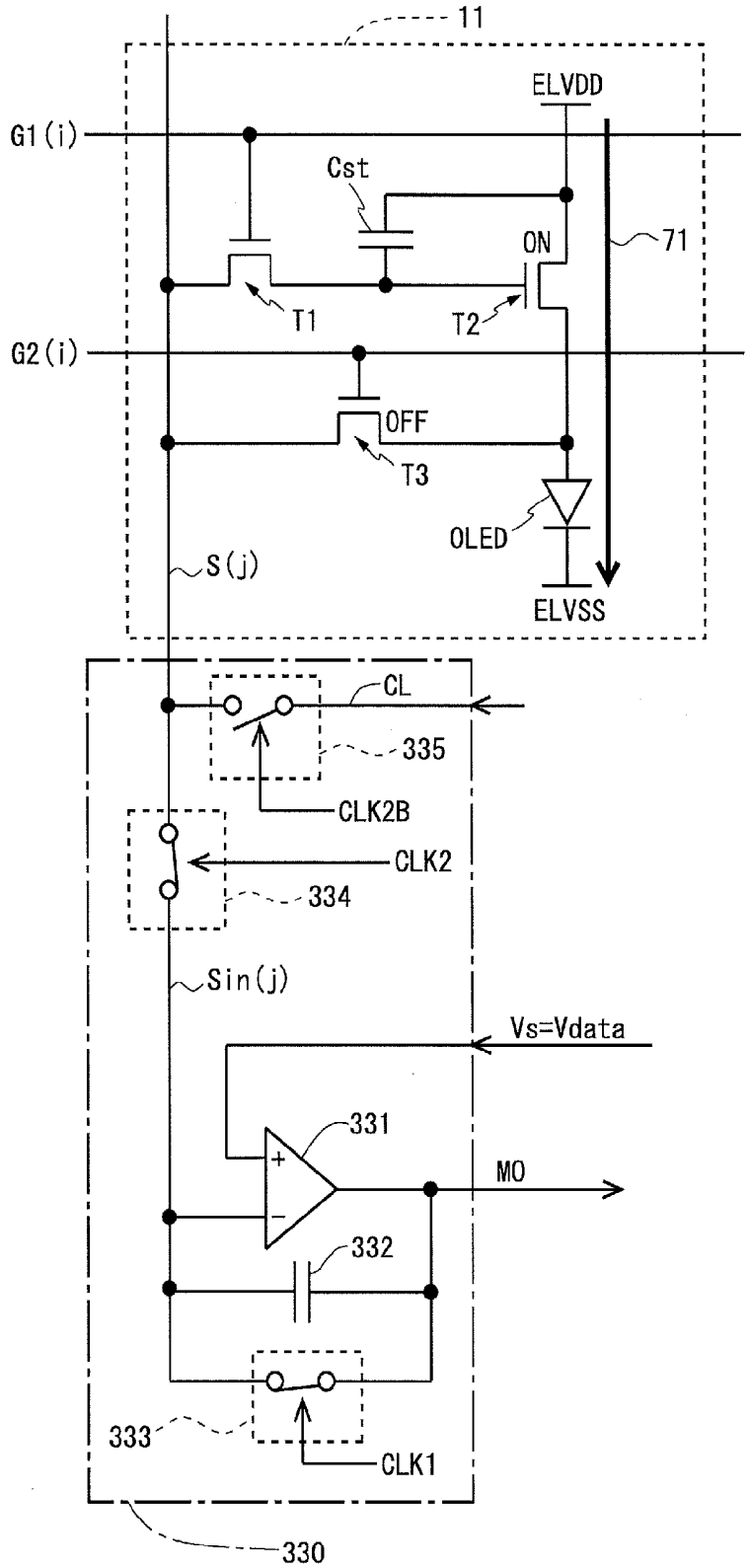

11
ELVDD
G1(i)
Cst
ON
71
T1
T2
G2(i)
OFF
T3
OLED
S(j)
ELVSS
CL
335
CLK2B
CLK2
334
Sin(j)
Vs=Vdata
331
MO
332
333
CLK1
330

Fig.12

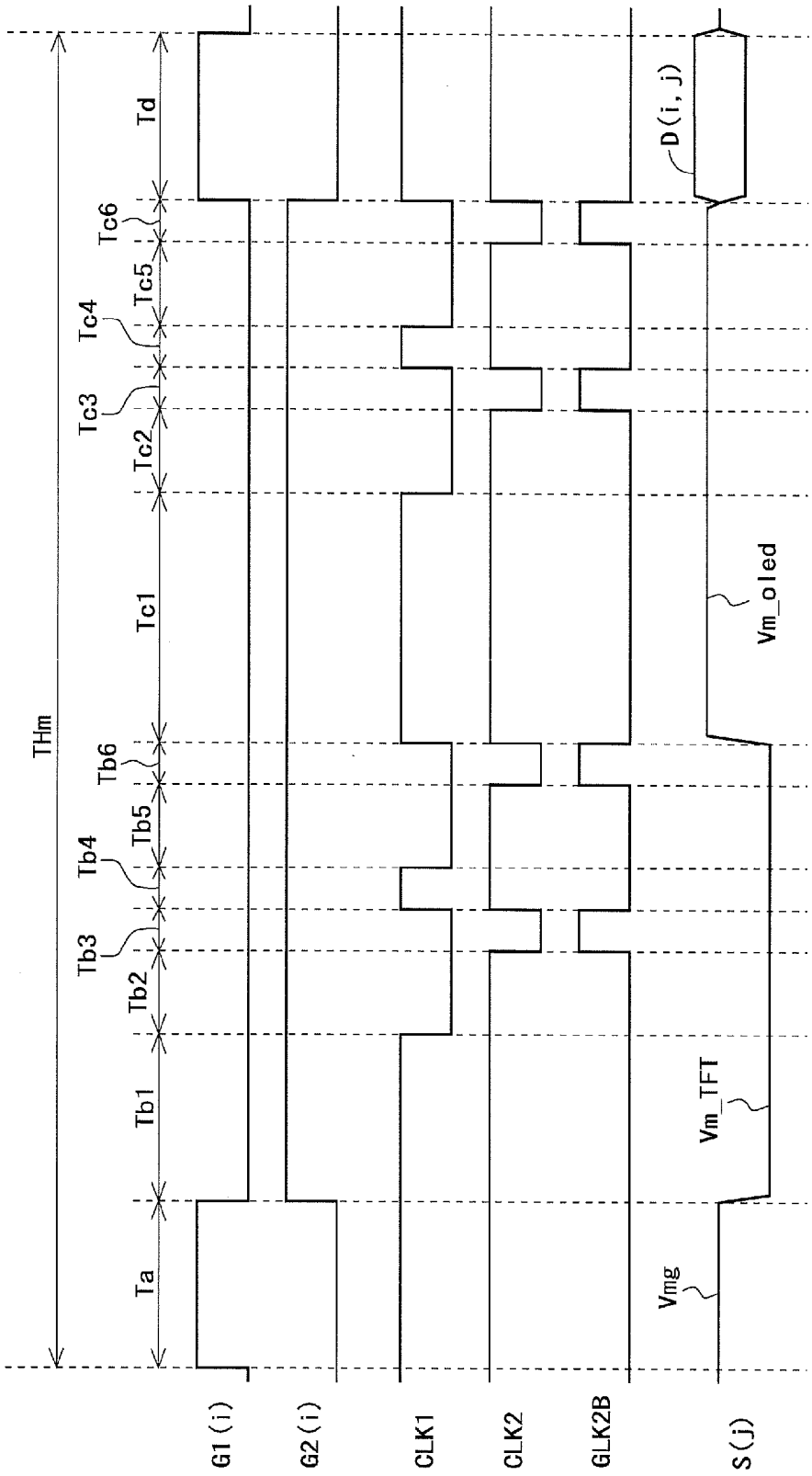

THm
Ta
Tb1
Tb2
Tb3
Tb4
Tb5
Tb6
Tc1
Tc2
Tc3
Tc4
Tc5
Tc6
Td
G1(i)
G2(i)
CLK1
CLK2
GLK2B
S(j)
Vmg
Vm_TFT
Vm_oled
D(i, j)

Fig.13

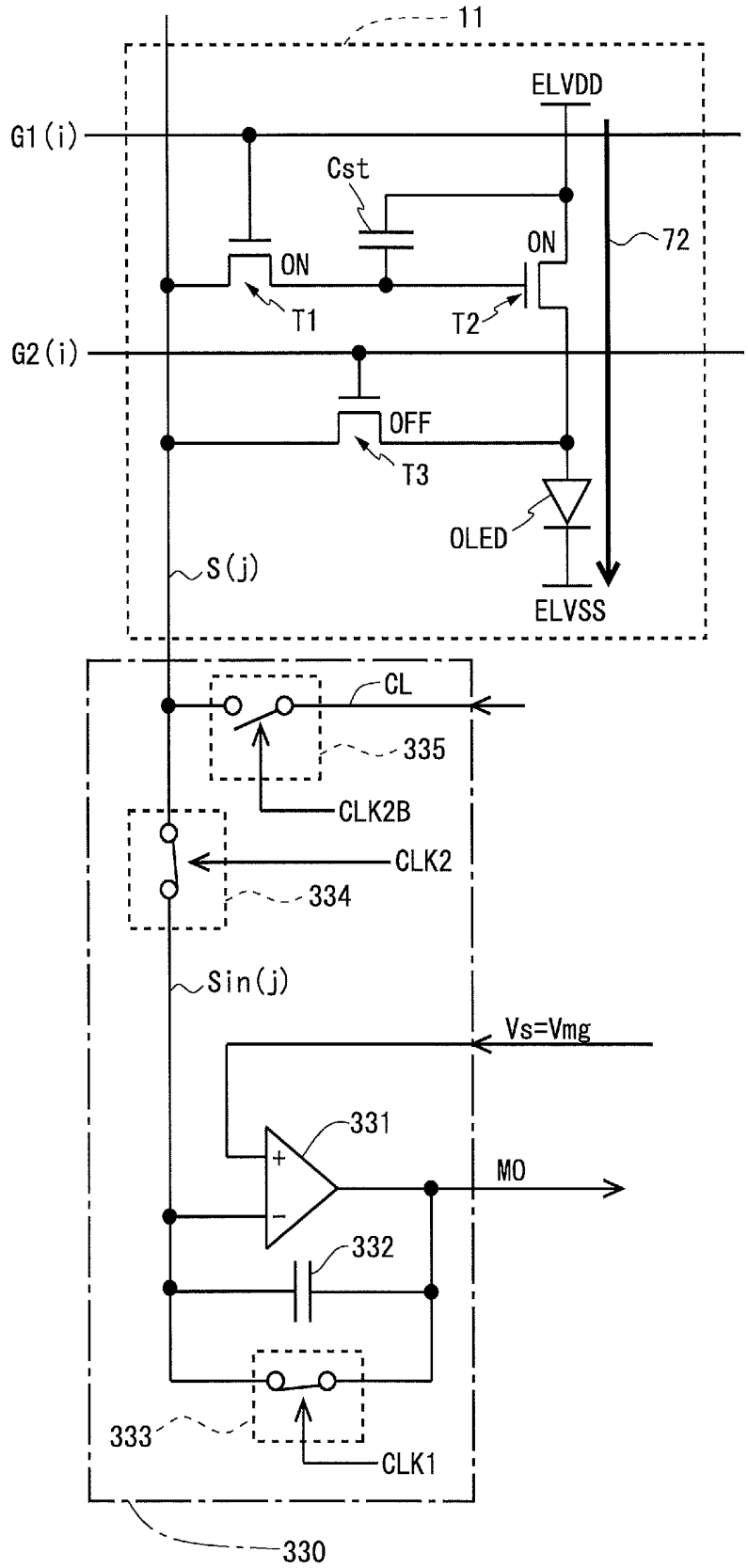

11
ELVDD
G1(i)
Cst
ON
ON
72
T1
T2
G2(i)
OFF
T3
OLED
S(j)
ELVSS
CL
335
CLK2B
CLK2
334
Sin(j)
Vs=Vmg
331
MO
332
333
CLK1
330

Fig.14

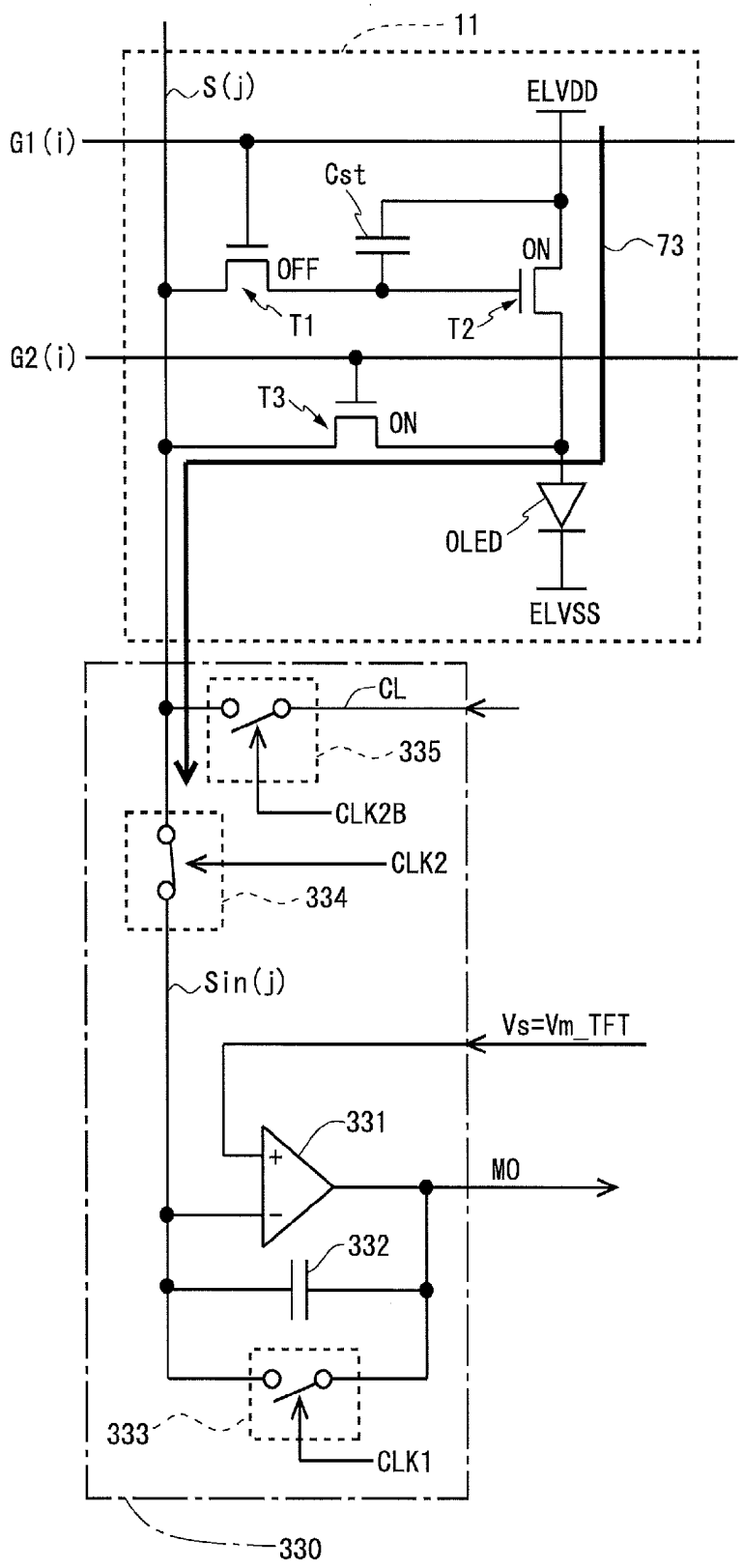

11
S(j)
ELVDD
G1(i)
Cst
73
ON
OFF
T1
T2
G2(i)
T3
ON
OLED
ELVSS
CL
335
CLK2B
CLK2
334
Sin(j)
Vs=Vm_TFT
331
MO
332
333
CLK1
330

Fig.15

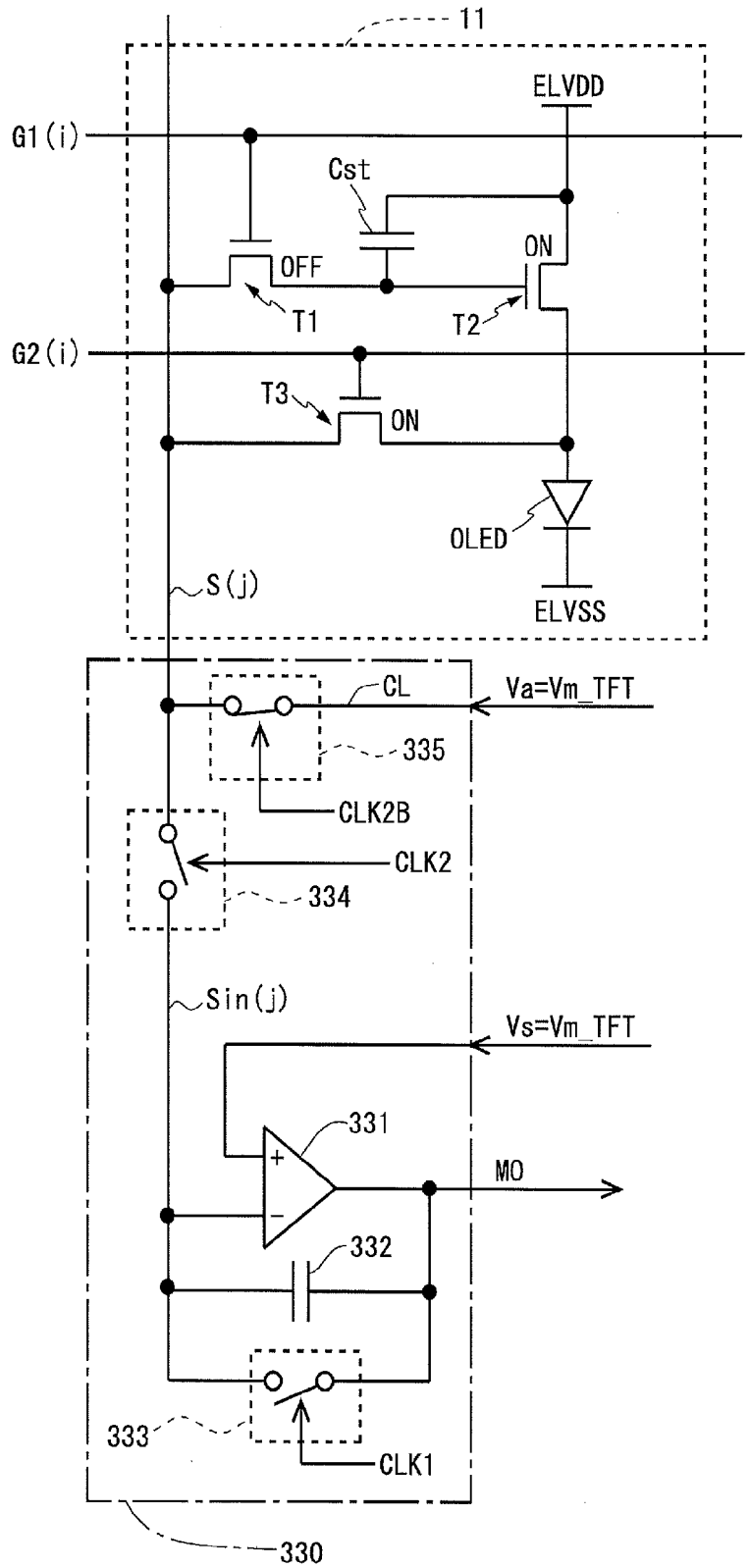

11
ELVDD
G1(i)
Cst
ON
OFF
T1
T2
G2(i)
T3
ON
OLED
S(j)
ELVSS
CL
Va=Vm_TFT
335
CLK2B
CLK2
334
Sin(j)
Vs=Vm_TFT
331
MO
332
333
CLK1
330

Fig.16

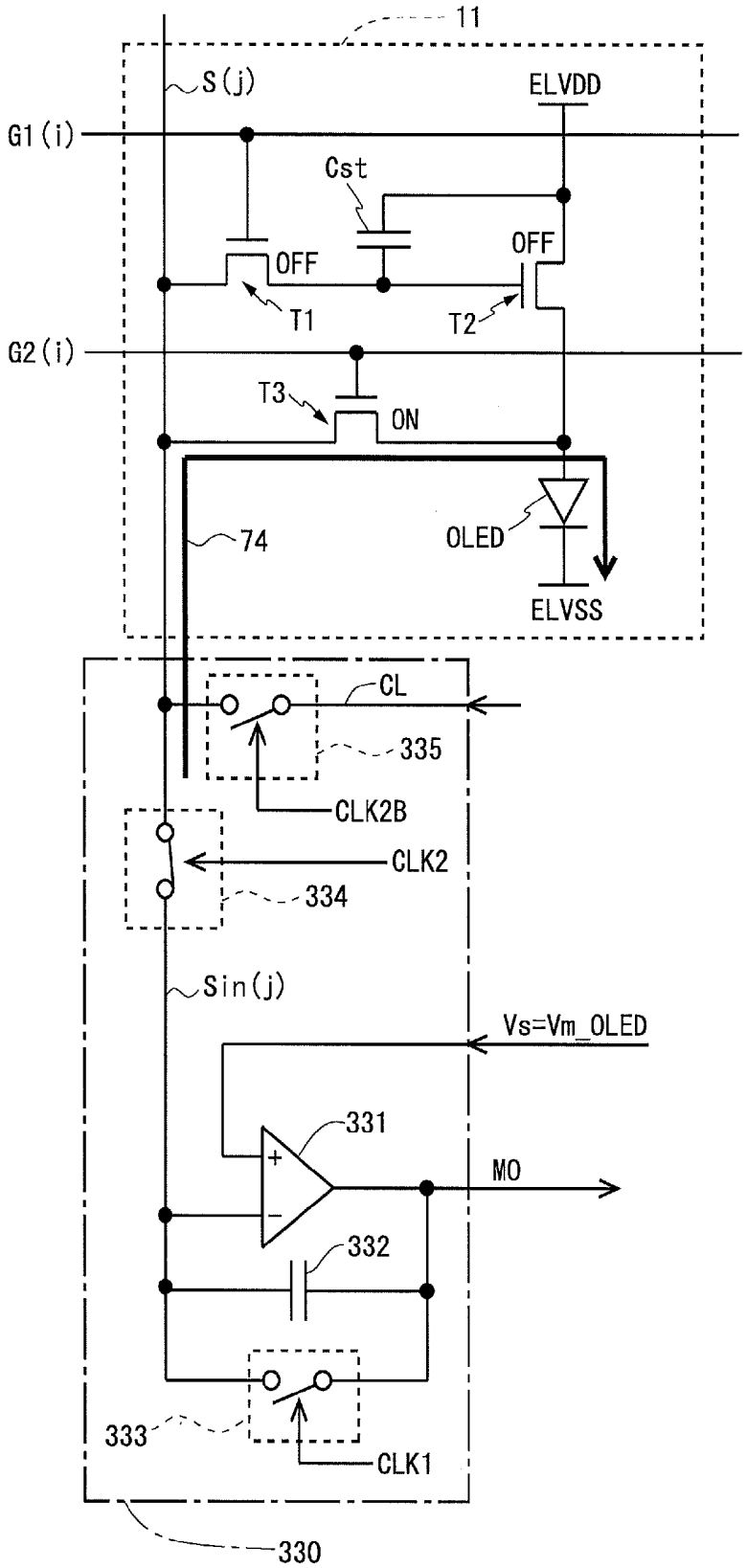

11
S(j)
ELVDD
G1(i)
Cst
OFF
OFF
T1
T2
G2(i)
T3
ON
74
OLED
ELVSS
CL
335
CLK2B
CLK2
334
Sin(j)
Vs=Vm_OLED
331
MO
332
333
CLK1
330

Fig.17

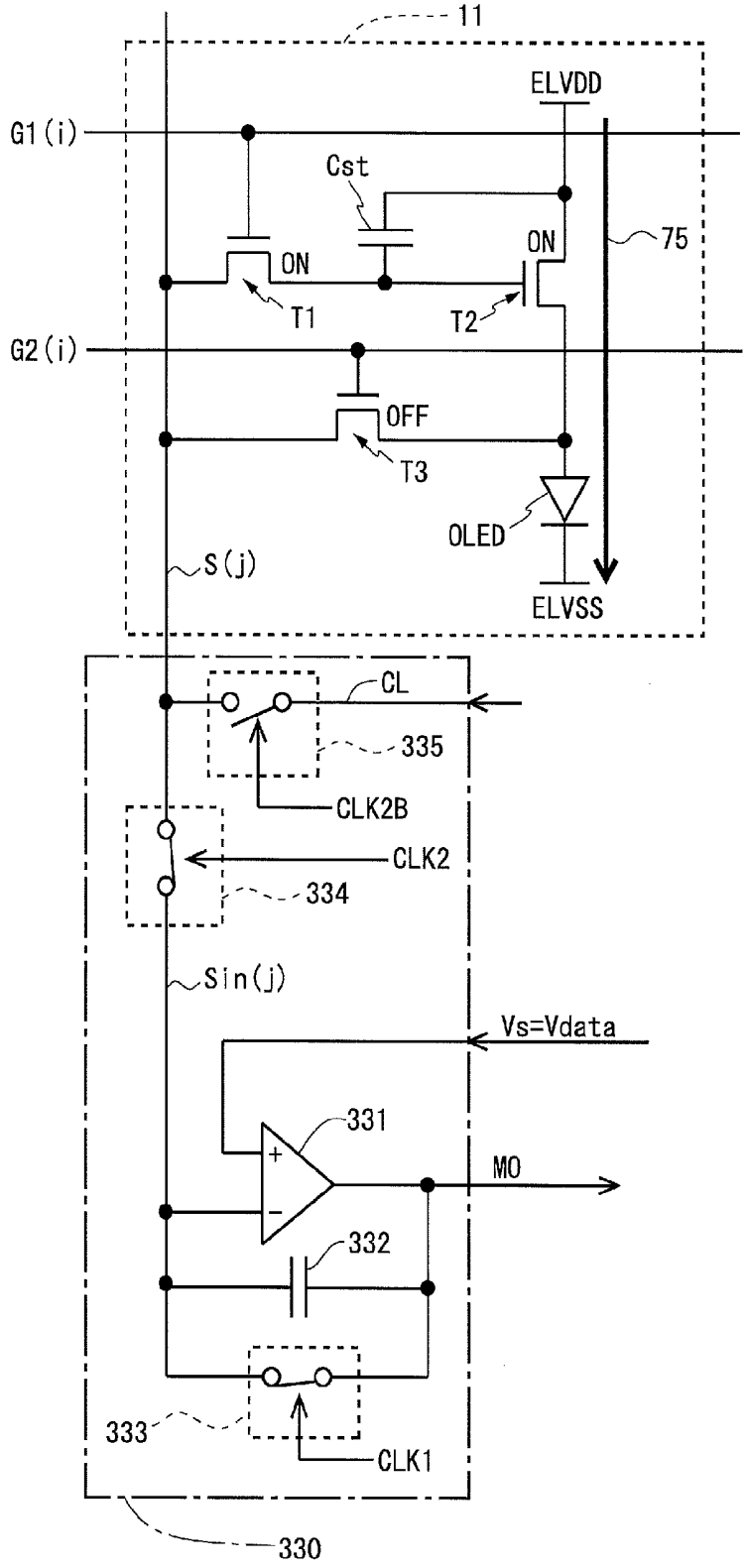

11
ELVDD
G1(i)
Cst
ON
ON
75
T1
T2
G2(i)
OFF
T3
OLED
S(j)
ELVSS
CL
335
CLK2B
CLK2
334
Sin(j)
Vs=Vdata
331
MO
332
333
CLK1
330

Fig.18

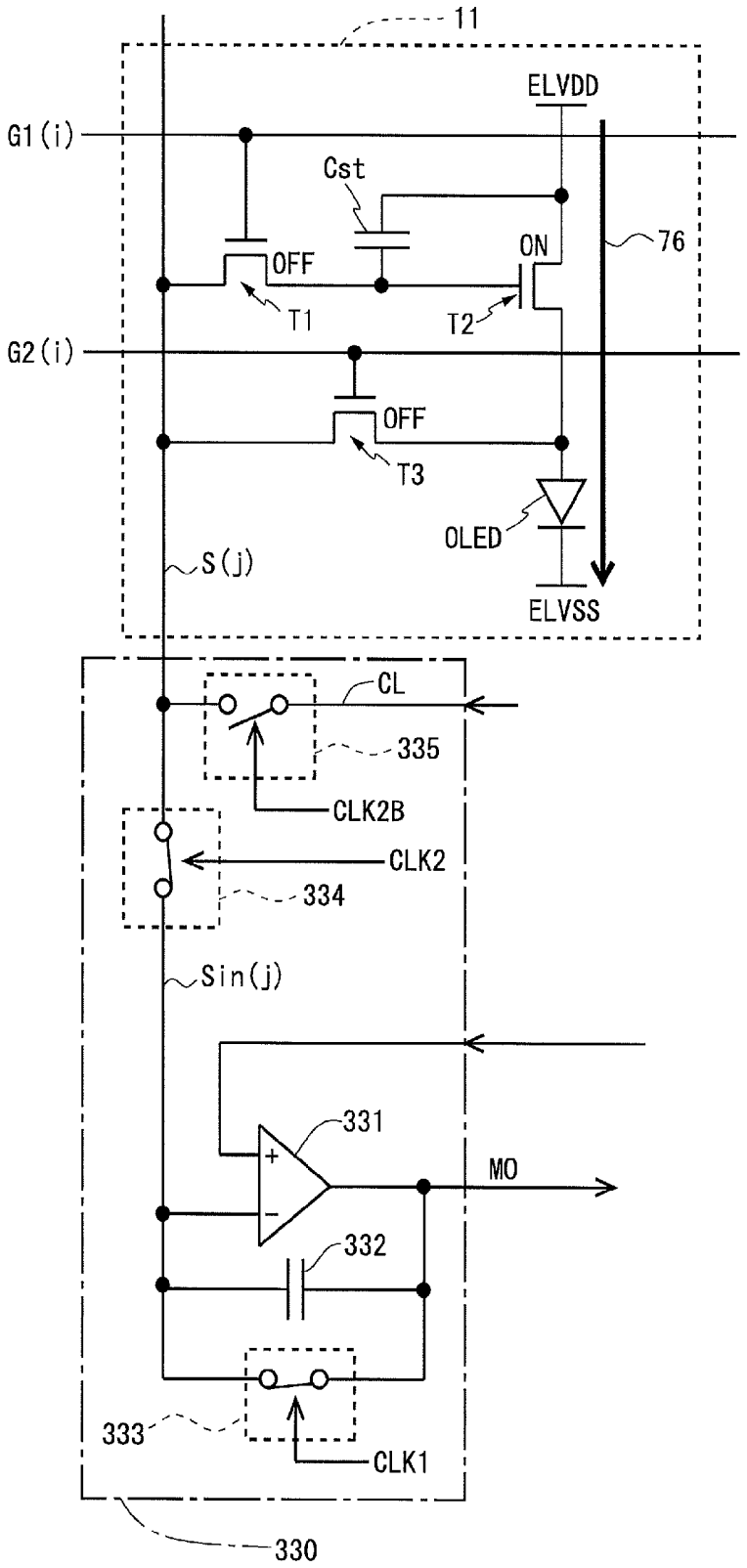

11
ELVDD
G1(i)
Cst
OFF
ON
76
T1
T2
G2(i)
OFF
T3
OLED
S(j)
ELVSS
CL
335
CLK2B
CLK2
334
Sin(j)
331
MO
332
333
CLK1
330

Fig.19

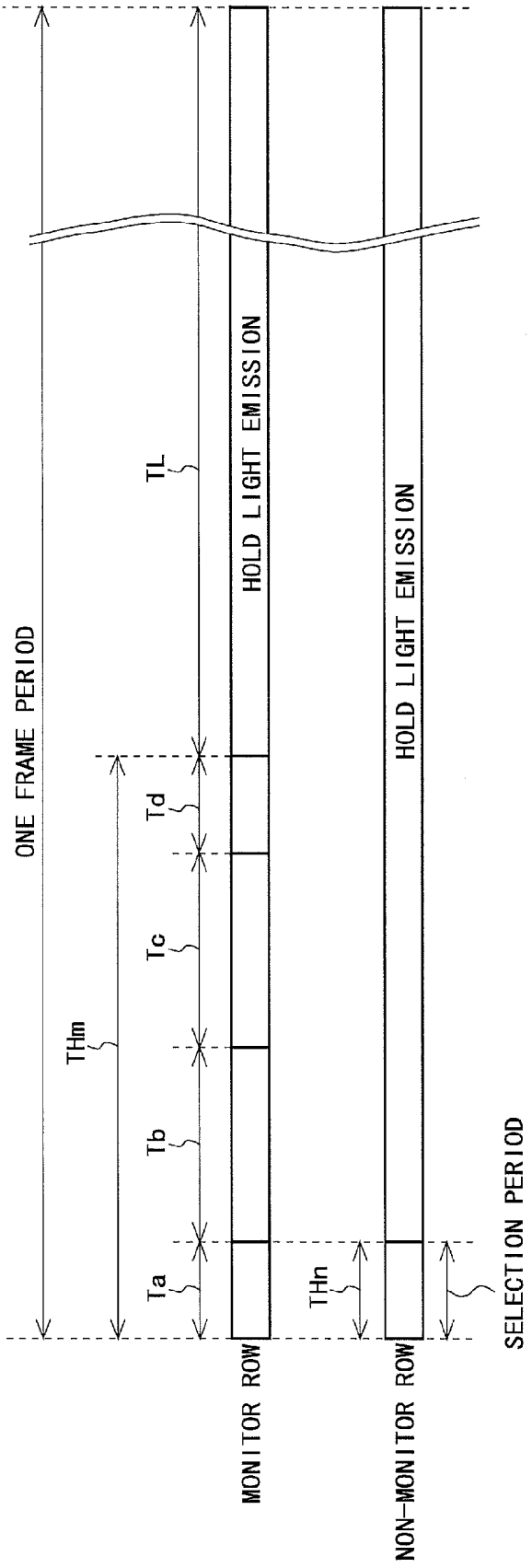

ONE FRAME PERIOD
TL
HOLD LIGHT EMISSION
HOLD LIGHT EMISSION
Td
Tc
THm
Tb
Ta
THn
SELECTION PERIOD
MONITOR ROW
NON-MONITOR ROW

Fig.20

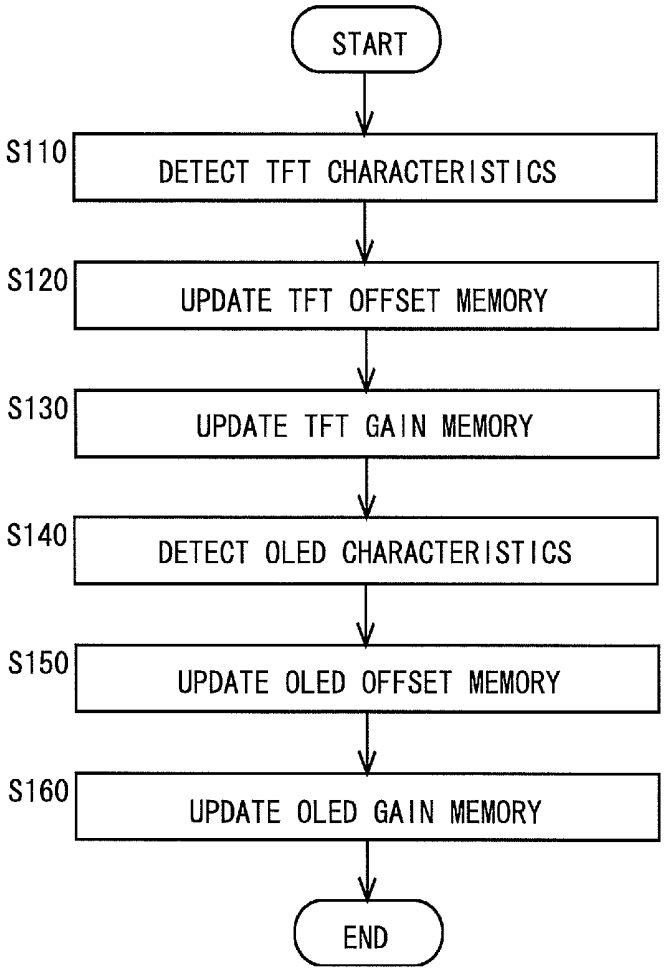

START
S110
DETECT TFT CHARACTERISTICS
S120
UPDATE TFT OFFSET MEMORY
S130
UPDATE TFT GAIN MEMORY
S140
DETECT OLED CHARACTERISTICS
S150
UPDATE OLED OFFSET MEMORY
S160
UPDATE OLED GAIN MEMORY
END

Fig.21

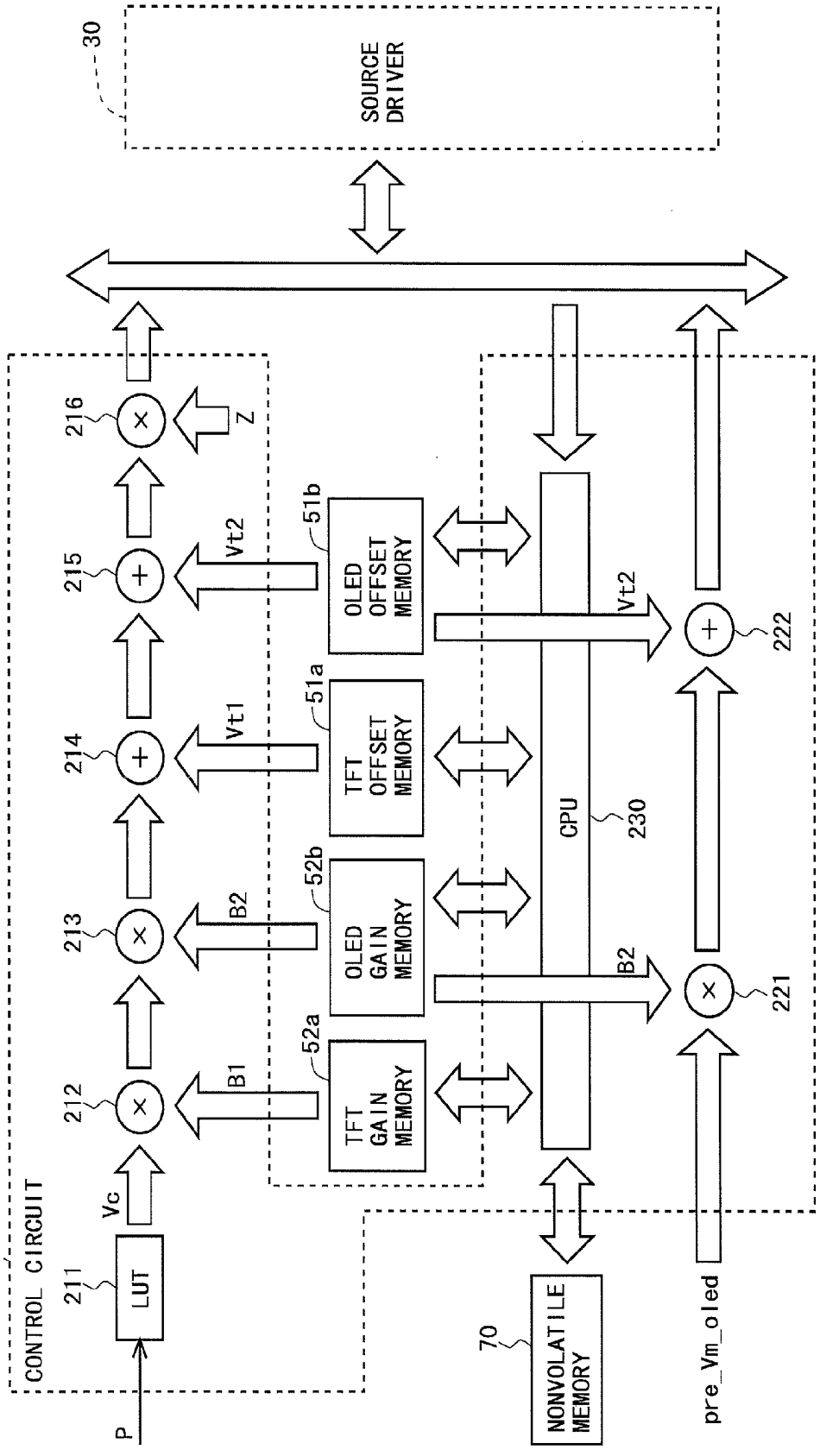

30
SOURCE DRIVER
20
CONTROL CIRCUIT
211
LUT
P
Vc
212
213
214
215
216
B1
B2
Vt1
Vt2
Z
52a
TFT GAIN MEMORY
52b
OLED GAIN MEMORY
51a
TFT OFFSET MEMORY
51b
OLED OFFSET MEMORY
CPU
230
221
222
70
NONVOLATILE MEMORY
pre_Vm_oled

Fig.22

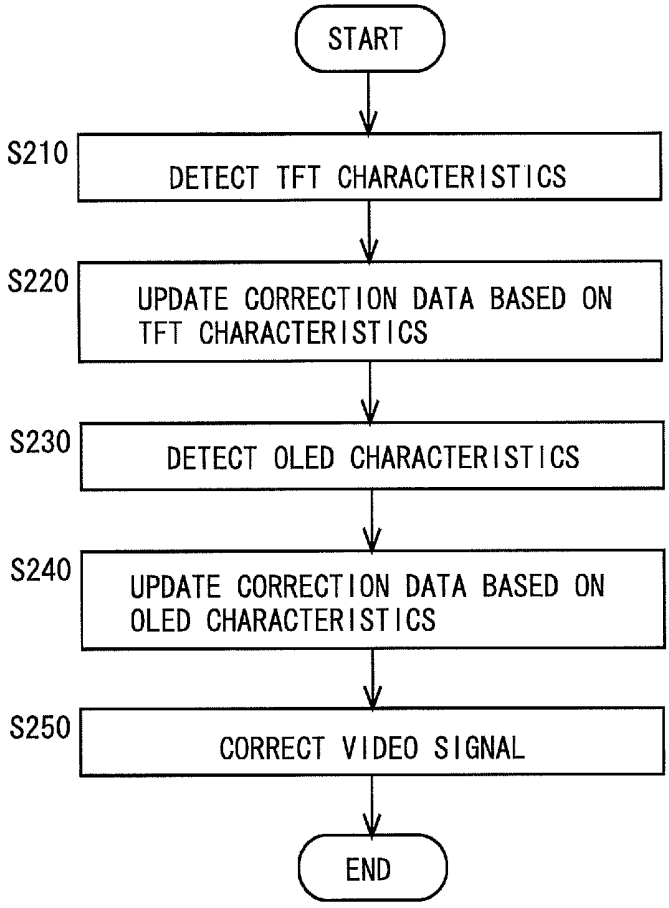

START
S210
DETECT TFT CHARACTERISTICS
S220
UPDATE CORRECTION DATA BASED ON TFT CHARACTERISTICS
S230
DETECT OLED CHARACTERISTICS
S240
UPDATE CORRECTION DATA BASED ON OLED CHARACTERISTICS
S250
CORRECT VIDEO SIGNAL
END

Fig.23

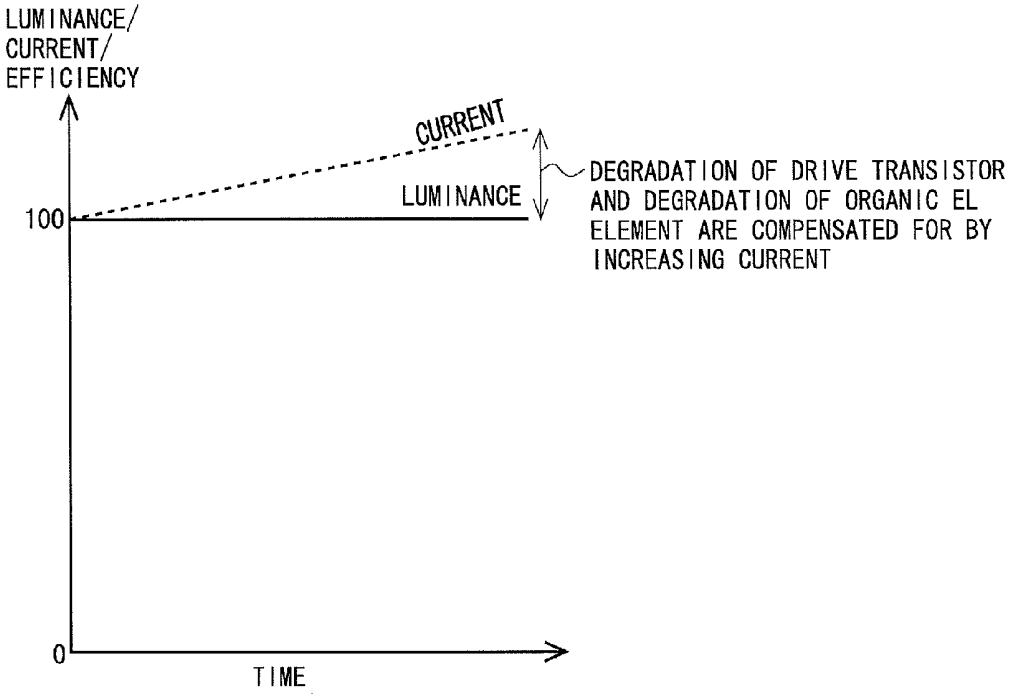

LUMINANCE/
CURRENT/
EFFICIENCY
CURRENT
LUMINANCE
100
0
TIME
DEGRADATION OF DRIVE TRANSISTOR AND DEGRADATION OF ORGANIC EL ELEMENT ARE COMPENSATED FOR BY INCREASING CURRENT

Fig.24

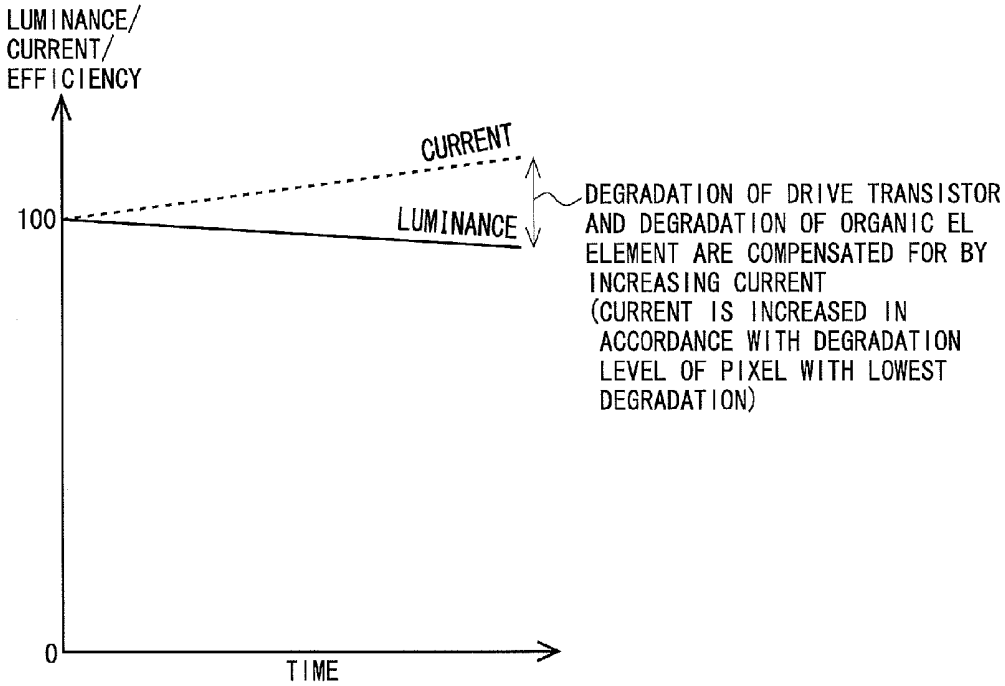

LUMINANCE/
CURRENT/
EFFICIENCY
CURRENT
LUMINANCE
100
0
TIME
DEGRADATION OF DRIVE TRANSISTOR AND DEGRADATION OF ORGANIC EL ELEMENT ARE COMPENSATED FOR BY INCREASING CURRENT (CURRENT IS INCREASED IN ACCORDANCE WITH DEGRADATION LEVEL OF PIXEL WITH LOWEST DEGRADATION)

Fig.25

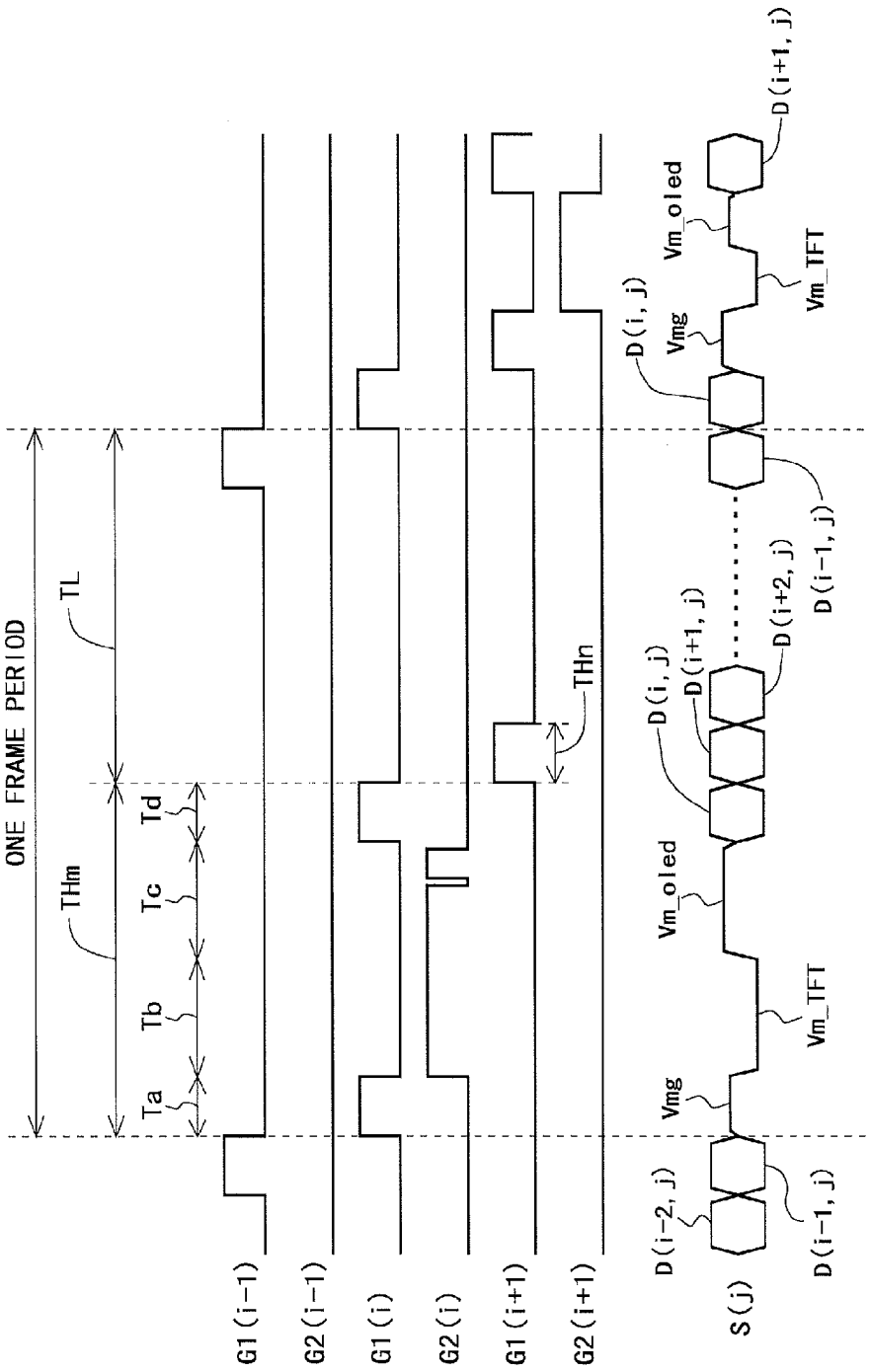

ONE FRAME PERIOD
TL
THm
Ta
Tb
Tc
Td
THn
G1 (i−1)
G2 (i−1)
G1 (i)
G2 (i)
G1 (i+1)
G2 (i+1)
S (j)
D (i−2, j)
D (i−1, j)
D (i, j)
D (i+1, j)
D (i+2, j)
Vmg
Vm_oled
Vm_TFT

Fig.26

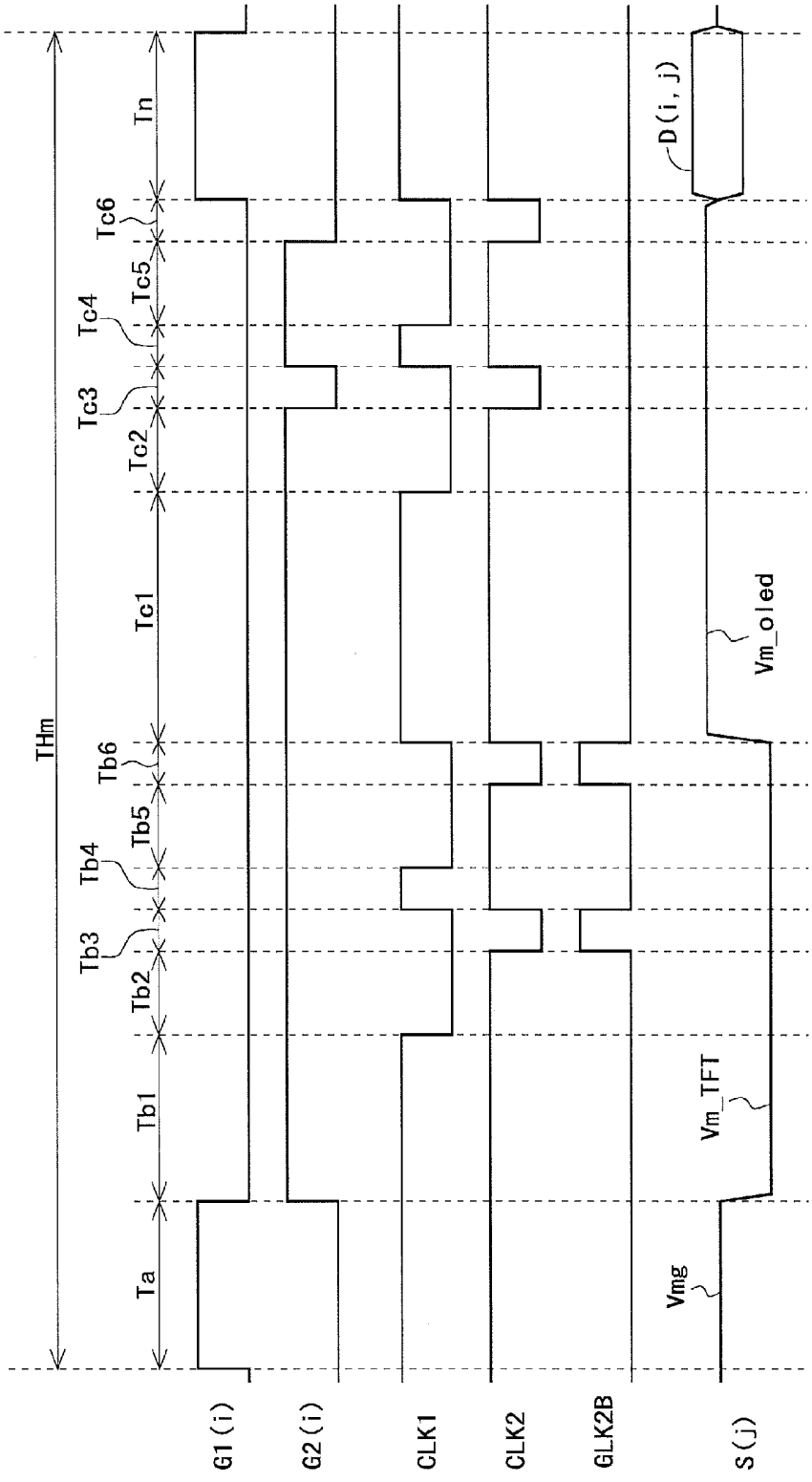

THm
Ta
Tb1
Tb2
Tb3
Tb4
Tb5
Tb6
Tc1
Tc2
Tc3
Tc4
Tc5
Tc6
Tn
G1(i)
G2(i)
CLK1
CLK2
GLK2B
S(j)
Vmg
Vm_TFT
Vm_oled
D(i, j)

Fig.27

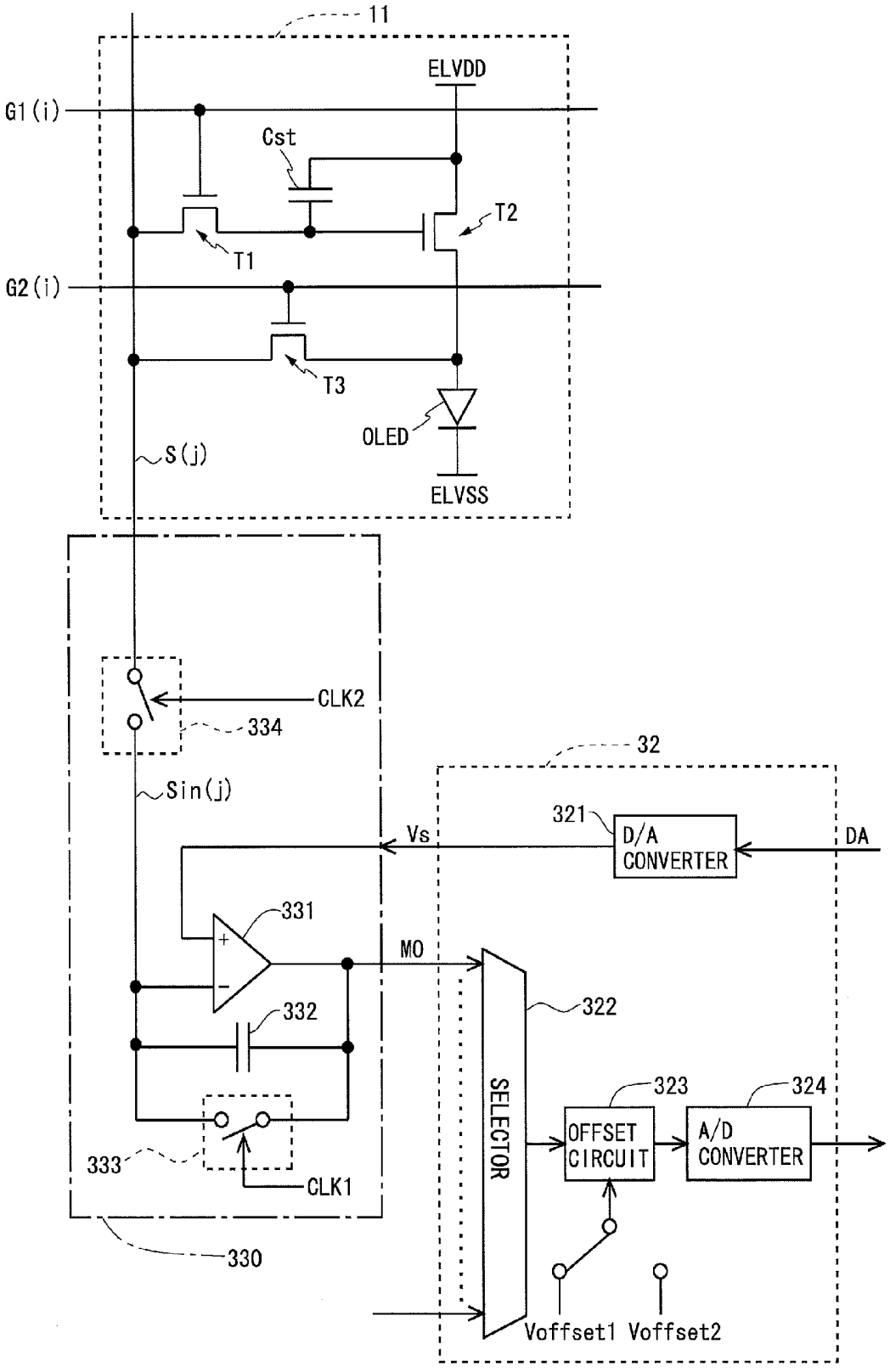

11
ELVDD
G1(i)
Cst
T2
T1
G2(i)
T3
OLED
S(j)
ELVSS
CLK2
334
32
Sin(j)
321
D/A CONVERTER
DA
Vs
331
MO
322
332
SELECTOR
323
324
OFFSET CIRCUIT
A/D CONVERTER
333
CLK1
330
Voffset1
Voffset2

Fig.28

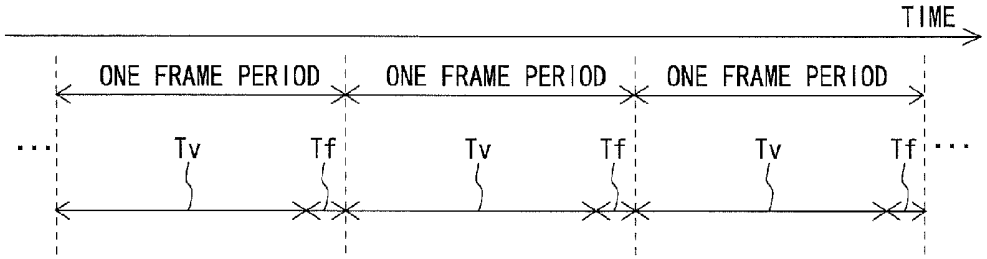

TIME
ONE FRAME PERIOD
ONE FRAME PERIOD
ONE FRAME PERIOD
Tv
Tf
Tv
Tf
Tv
Tf

Fig.29

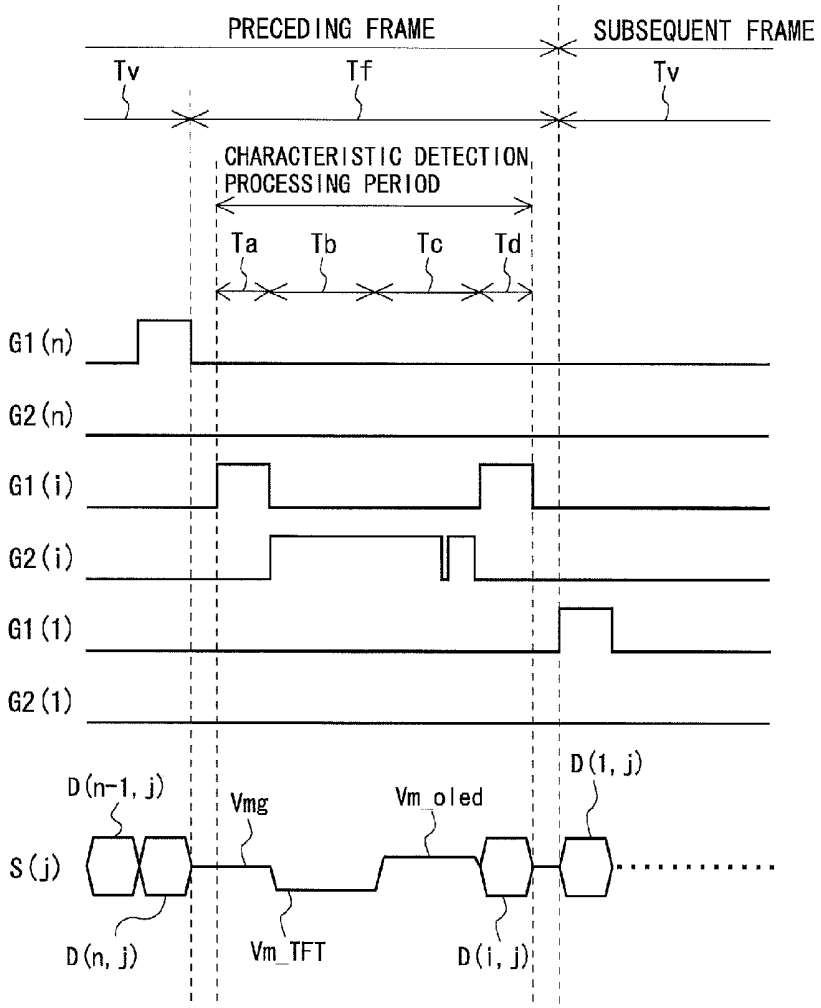

PRECEDING FRAME
SUBSEQUENT FRAME
Tv
Tf
Tv
CHARACTERISTIC DETECTION PROCESSING PERIOD
Ta
Tb
Tc
Td
G1(n)
G2(n)
G1(i)
G2(i)
G1(1)
G2(1)
D(n-1, j)
Vmg
Vm_oled
D(1, j)
S(j)
D(n, j)
Vm_TFT
D(i, j)

Fig.30

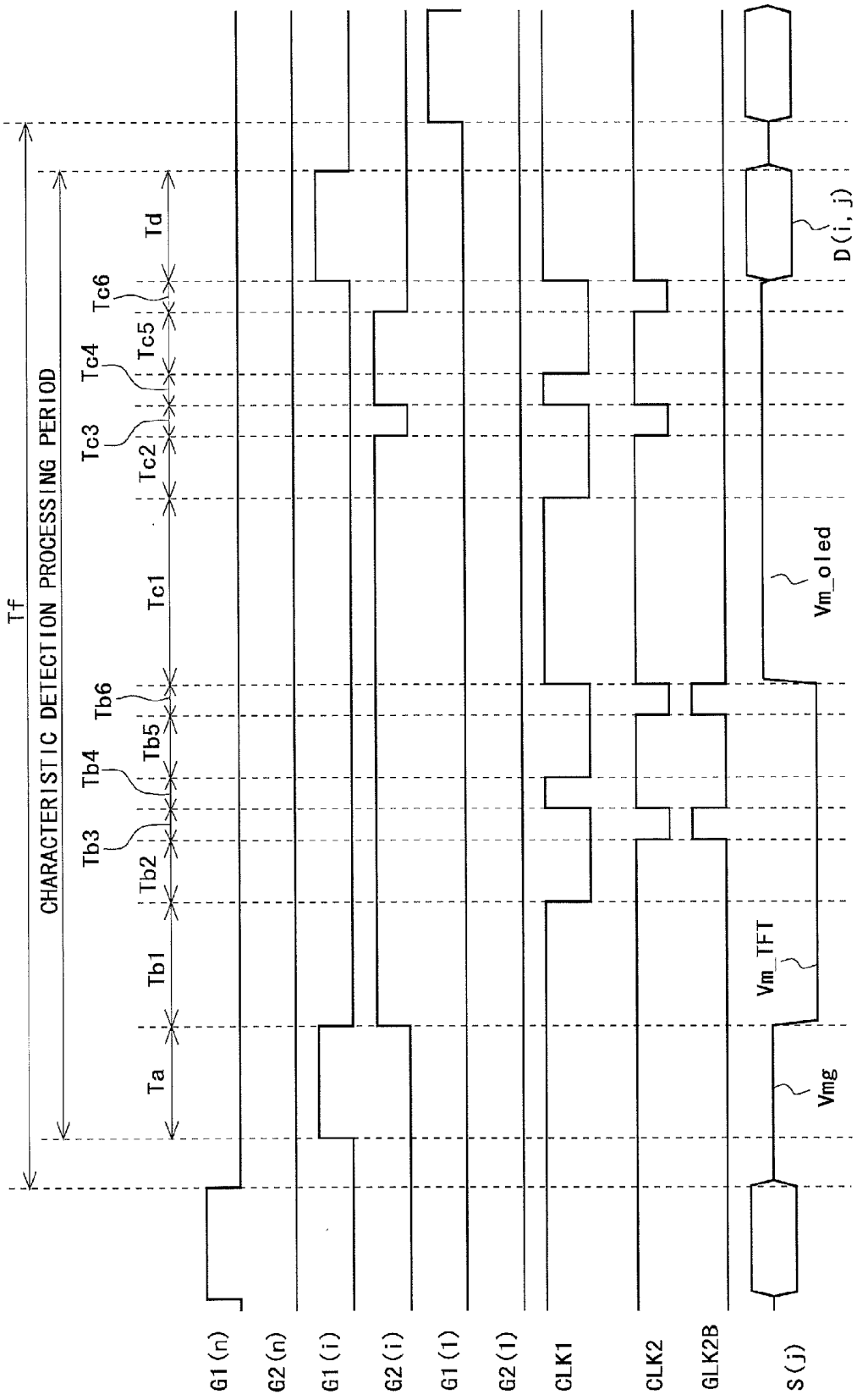

Tf
CHARACTERISTIC DETECTION PROCESSING PERIOD
Ta
Tb1
Tb2
Tb3
Tb4
Tb5
Tb6
Tc1
Tc2
Tc3
Tc4
Tc5
Tc6
Td
G1(n)
G2(n)
G1(i)
G2(i)
G1(1)
G2(1)
CLK1
CLK2
GLK2B
S(j)
Vmg
Vm_TFT
Vm_oled
D(i, j)

Fig.31

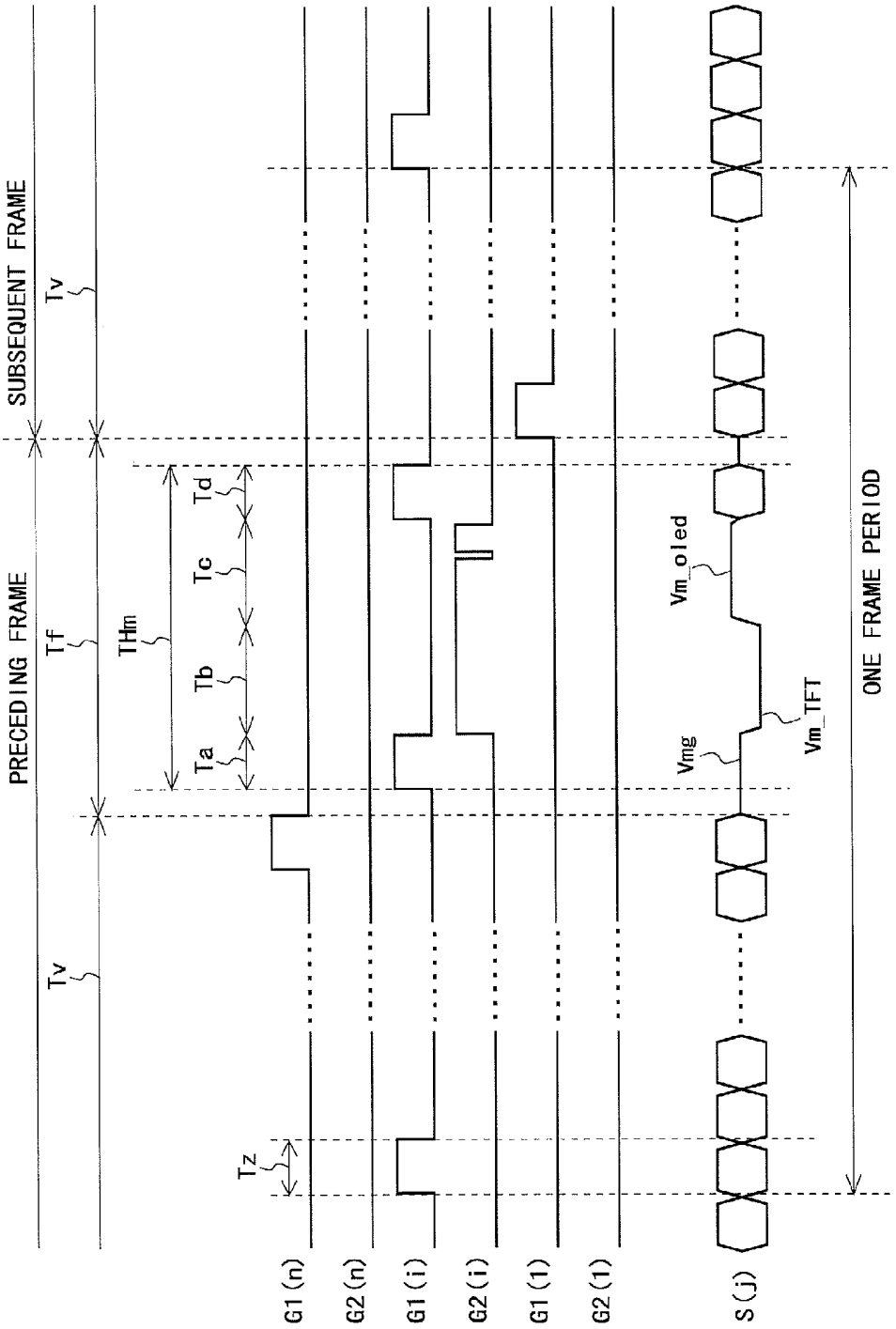

SUBSEQUENT FRAME
PRECEDING FRAME
Tv
Tf
THm
Td
Tc
Tb
Ta
Tz
Vm_oled
Vmg
Vm_TFT
ONE FRAME PERIOD
G1(n)
G2(n)
G1(i)
G2(i)
G1(1)
G2(1)
S(j)

Fig.32

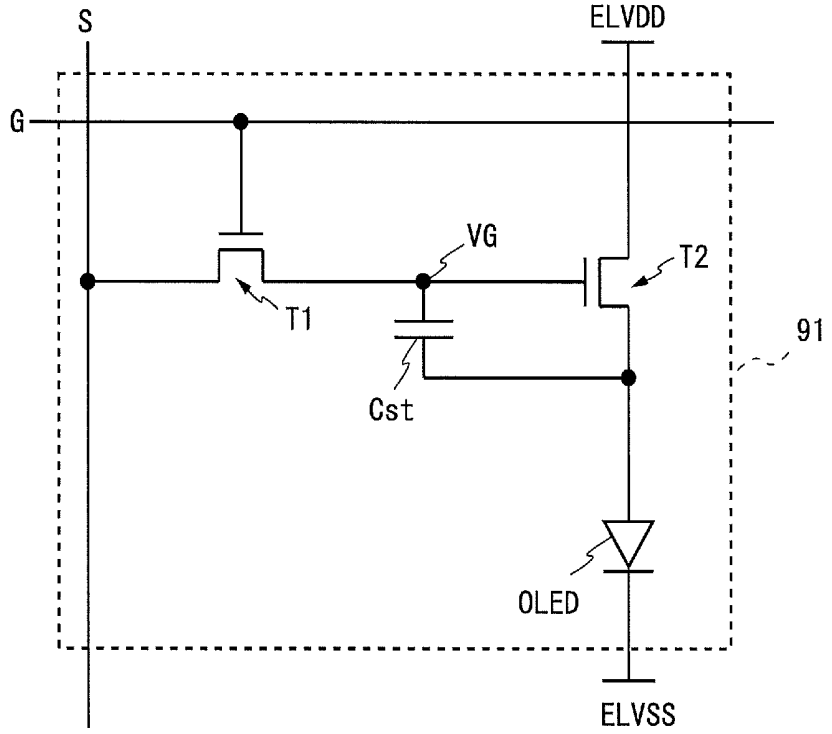

S
ELVDD
G
VG
T2
T1
91
Cst
OLED
ELVSS

Fig.33

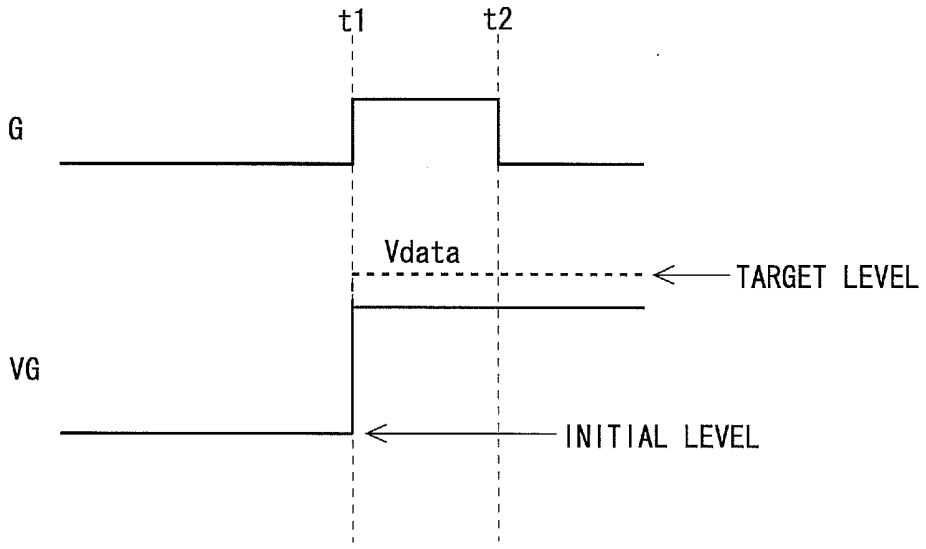

t1
t2
G
Vdata
TARGET LEVEL
VG
INITIAL LEVEL

Fig.34

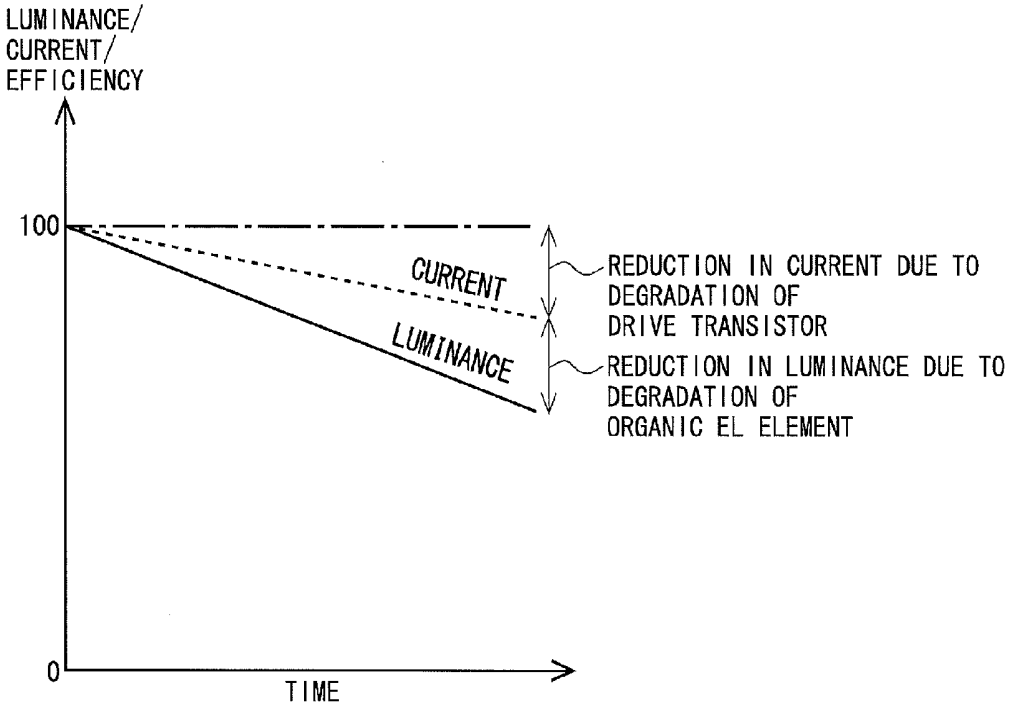

LUMINANCE/
CURRENT/
EFFICIENCY
100
0
CURRENT
LUMINANCE
TIME
REDUCTION IN CURRENT DUE TO DEGRADATION OF DRIVE TRANSISTOR
REDUCTION IN LUMINANCE DUE TO DEGRADATION OF ORGANIC EL ELEMENT

Fig.35

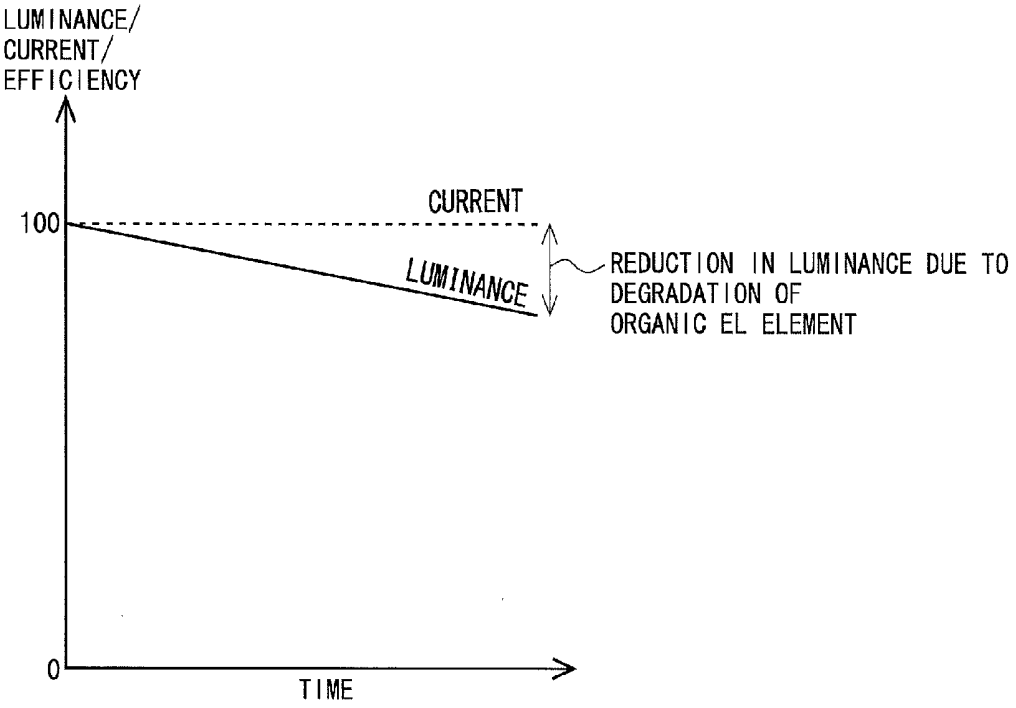
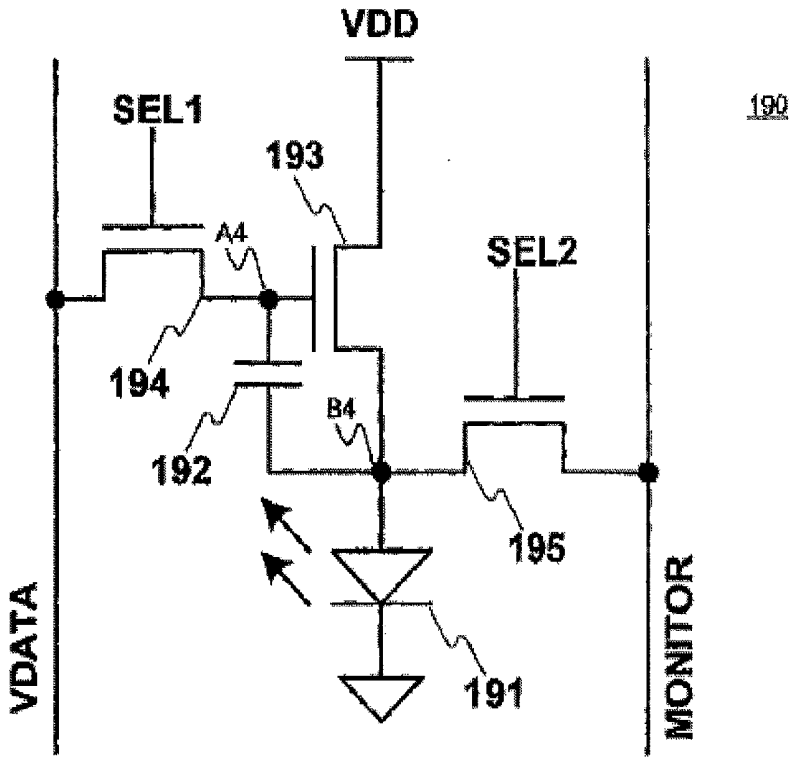

LUMINANCE/
CURRENT/
EFFICIENCY
100
0
CURRENT
LUMINANCE
TIME
REDUCTION IN LUMINANCE DUE TO DEGRADATION OF ORGANIC EL ELEMENT

Fig.36



DISPLAY DEVICE AND METHOD FOR DRIVING SAME

TECHNICAL FIELD

[0001] The present invention relates to a display device and a method for driving the same, and more specifically to a display device provided with a pixel circuit including an electrooptical element such as an organic EL (Electro Luminescence) element, and a method for driving the same.

BACKGROUND ART

[0002] As a display element provided in a display device, there have hitherto been an electrooptical element whose luminance is controlled by an applied voltage, and an electrooptical element whose luminance is controlled by a flowing current. Examples of the electrooptical element whose luminance is controlled by an applied voltage include a liquid crystal display element. Meanwhile, examples of the electrooptical element whose luminance is controlled by a flowing current include an organic EL element. The organic EL element is also called an OLED (Organic Light-Emitting Diode). An organic EL display device that uses the organic EL element being a spontaneous electrooptical element can be easily reduced in thickness and power consumption and increased in luminance as compared to the liquid crystal display device that requires a backlight, a color filter and the like. Hence in recent years, development of the organic EL display device has been actively advanced.

[0003] As drive systems for the organic EL display device, a passive matrix system (also called simple matrix system) and an active matrix system are known. As for an organic EL display device employing the passive matrix system, its structure is simple, but a large size and high definition are difficult to achieve. In contrast, as for an organic EL display device employing the active matrix system (hereinafter referred to as an "active matrix-type organic EL display device"), a large size and high definition can be easily realized as compared to the organic EL display device employing the passive matrix system.

[0004] In the active matrix-type organic EL display device, a plurality of pixel circuits are formed in a matrix form. The pixel circuit of the active matrix-type organic EL display device typically includes an input transistor for selecting a pixel and a drive transistor for controlling supply of a current to the organic EL element. It is to be noted that in the following, a current that flows from the drive transistor to the organic EL element may be referred to as a "drive current".

[0005] FIG. **32** is a circuit diagram showing a configuration of a conventional general pixel circuit **91**. This pixel circuit **91** is provided corresponding to each of intersections of a plurality of data lines S and a plurality of scanning lines G which are disposed in a display portion. As shown in FIG. **32**, this pixel circuit **91** is provided with two transistors T**1** and T**2**, one capacitor Cst, and one organic EL element OLED. The transistor T**1** is an input transistor, and the transistor T**2** is a drive transistor.

[0006] The transistor T**1** is provided between the data signal line S and a gate terminal of the transistor T**2**. As for the transistor T**1**, agate terminal is connected to the scanning line G, and a source terminal is connected to the data signal line S. The transistor T**2** is provided in series with the organic EL element OLED. As for the transistor T**2**, a drain terminal is connected to a power supply line that supplies a high-level power supply voltage ELVDD, and a source terminal is connected to an anode terminal of the organic EL element OLED. It should be noted that, the power supply line that supplies the high-level power supply voltage ELVDD is referred to as a "high-level power supply line" in the following, and the high-level power supply line is added with the same symbol ELVDD as that of the high-level power supply voltage. As for the capacitor Cst, one end is connected to the gate terminal of the transistor T**2**, and the other end is connected to the source terminal of the transistor T**2**. A cathode terminal of the organic EL element OLED is connected to a power supply line that supplies a low-level power supply voltage ELVSS. It should be noted that, the power supply line that supplies the low-level power supply voltage ELVSS is referred to as a "low-level power supply line" in the following, and the low-level power supply line is added with the same symbol ELVSS as that of the low-level power supply voltage. Further, here, a contact point of the gate terminal of the transistor T**2**, the one end of the capacitor Cst, and the drain terminal of the transistor T**1** is referred to as a "gate node VG" for the sake of convenience. It is to be noted that, although one having a higher potential between a drain and a source is generally called a drain, in descriptions of the present specification, one is defined as a drain and the other is defined as a source, and hence a source potential may become higher than a drain potential.

[0007] FIG. **33** is a timing chart for explaining an operation of the pixel circuit **91** shown in FIG. **32**. Before time t**1**, the scanning line G is in a non-selected state. Therefore, before the time t**1**, the transistor T**1** is in an off state, and a potential of the gate node VG is held at an initialization level (e.g., a level in accordance with writing in the last frame). At the time t**1**, the scanning line G comes into a selected state and the transistor T**1** is turned on. Thereby, a data voltage Vdata corresponding to a luminance of a pixel (sub-pixel) formed by this pixel circuit **91** is supplied to the gate node VG via the data signal line S and the transistor T**1**. Thereafter, in a period till time t**2**, the potential of the gate node VG changes in accordance with the data voltage Vdata. At this time, the capacitor Cst is charged with a gate-source voltage Vgs which is a difference between the potential of the gate node VG and a source potential of the transistor T**2**. At the time t**2**, the scanning line G comes into the non-selected state. Thereby, the transistor T**1** is turned off and the gate-source voltage Vgs held by the capacitor Cst is determined. The transistor T**2** supplies a drive current to the organic EL element OLED in accordance with the gate-source voltage Vgs held by the capacitor Cst. As a result, the organic EL element OLED emits light with a luminance in accordance with the drive current.

[0008] Incidentally, in the organic EL display device, a thin film transistor (TFT) is typically employed as the drive transistor. However, regarding the thin film transistor, variations in threshold voltage tend to occur. When variations in threshold voltage occur in the drive transistor provided in the display portion, variations in luminance occur, and the display quality thus deteriorates. Accordingly, a technique of suppressing deterioration in display quality in the organic EL display device has hitherto been proposed. For example, Japanese Patent Application Laid-Open No. 2005-31630 discloses a technique of compensating for variations in threshold voltage of a drive transistor. Further, Japanese

Patent Application Laid-Open No. 2003-195810 and Japanese Patent Application Laid-Open No. 2007-128103 each discloses a technique of making constant a current flowing from a pixel circuit to an organic EL element OLED. Moreover, Japanese Patent Application Laid-Open No. 2007-233326 discloses a technique of displaying an image with a uniform luminance regardless of electron mobility and a threshold voltage of a drive transistor.

[0009] According to the foregoing prior arts, even when variations in threshold voltage occur in the drive transistor provided in the display portion, it is possible to supply a constant current to the organic EL element (light-emitting element) in accordance with a desired luminance (target luminance). However, as for the organic EL element, current efficiency decreases with the lapse of time. That is, even when a constant current is supplied to the organic EL element, the luminance gradually decreases with the lapse of time. This results in occurrence of burning.

[0010] Thus, unless compensation is performed on degradation of the drive transistor and degradation of the organic EL element, current decrease due to the degradation of the drive transistor occurs and luminance decrease due to the degradation of the organic EL element occurs as shown in FIG. **34**. Further, even when compensation is performed on the degradation of the drive transistor, luminance decrease due to the degradation of the organic EL element occurs with the lapse of time as shown in FIG. **35**. Accordingly, Japanese Translation of PCT International Application Publication No. 2008-523448 discloses a technique of correcting data based on a characteristic of the organic EL element OLED in addition to the technique of correcting data based on a characteristic of the drive transistor.

PRIOR ART DOCUMENTS

Patent Documents

[0011] [Patent Document 1] Japanese Patent Application Laid-Open No. 2005-31630

[0012] [Patent Document 2] Japanese Patent Application Laid-Open No. 2003-195810

[0013] [Patent Document 3] Japanese Patent Application Laid-Open No. 2007-128103

[0014] [Patent Document 4] Japanese Patent Application Laid-Open No. 2007-233326

[0015] [Patent Document 5] Japanese Translation of PCT International Application Publication No. 2008-523448

SUMMARY OF THE INVENTION

Problems to be Solved by the Invention

[0016] However, according to the techniques disclosed in Japanese Translation of PCT International Application Publication No. 2008-523448, during a selection period, a characteristic of only either one of a drive transistor and an organic EL element can be detected. Hence, simultaneous compensation for both of degradation of the drive transistor and degradation of the organic EL element cannot be performed.

[0017] In addition, when a display device is configured to enable detection of a characteristic of a drive transistor and detection of a characteristic of an organic EL element, it is desired to minimize an increase in circuit size. This is because if the circuit size increases, it is disadvantageous in terms of, for example, achievement of low power consumption and achievement of miniaturization. Regarding this point, in the techniques disclosed in Japanese Translation of PCT International Application Publication No. 2008-523448, as shown in FIG. **36**, a current detection monitoring line MONITOR for characteristic detection is provided in addition to a data signal line VDATA for supplying a data signal to a pixel circuit. Hence, the degree of an increase in circuit size is large.

[0018] An object of the present invention is therefore to implement a display device capable of compensating for degradation of circuit elements while suppressing an increase in circuit size (particularly, a display device capable of simultaneously compensating for both of degradation of drive transistors and degradation of organic EL elements).

Means for Solving the Problems

[0019] A first aspect of the present invention is directed to an active matrix-type display device including:

[0020] a display unit having: a pixel matrix of n rows×m columns including n×m pixel circuits (n and m are integers greater than or equal to 2), each pixel circuit including an electrooptical element whose luminance is controlled by a current and a drive transistor for controlling a current to be supplied to the electrooptical element; scanning lines provided for the respective rows of the pixel matrix; monitoring control lines provided for the respective rows of the pixel matrix; and data signal lines provided for the respective columns of the pixel matrix;

[0021] a pixel circuit driving unit configured to drive the scanning lines, the monitoring control lines, and the data signal lines such that a characteristic detection process is performed during a frame period and that each electrooptical element emits light according to a target luminance, the characteristic detection process detecting a characteristic of a characteristic detection target circuit element including at least one of the electrooptical element and the drive transistor;

[0022] a correction data storage unit configured to store characteristic data obtained based on results of the characteristic detection process, as correction data for correcting video signals; and

[0023] a video signal correcting unit configured to generate data signals to be supplied to the n×m pixel circuits by correcting the video signals based on the correction data stored in the correction data storage unit, wherein

[0024] each of the pixel circuits includes:

[0025] the electrooptical element;

[0026] an input transistor having a control terminal connected to the scanning line, a first conduction terminal connected to a control terminal of the drive transistor, and a second conduction terminal connected to the data signal line;

[0027] the drive transistor having a first conduction terminal to which a drive power supply potential is provided;

[0028] a monitoring control transistor having a control terminal connected to the monitoring control line, a first conduction terminal connected to a second conduction terminal of the drive transistor and an anode of the electrooptical element, and a second conduction terminal connected to the data signal line; and

[0029] a first capacitor having one end connected to the control terminal of the drive transistor to hold a potential of the control terminal of the drive transistor,

[0030] the pixel circuit driving unit includes:

[0031] an output and current-monitoring circuit having a function of applying the data signal to the data signal line and a function of obtaining, as monitored data, data according to a magnitude of a current flowing through the data signal line, the monitored data being base data for the characteristic data; and

[0032] an AD conversion circuit configured to convert the monitored data from an analog value to a digital value,

[0033] the output and current-monitoring circuit includes:

[0034] an internal data line connected to the data signal line;

[0035] an operational amplifier having a non-inverting input terminal to which the data signal is provided, and an inverting input terminal connected to the internal data line;

[0036] a second capacitor having one end connected to the internal data line, and an other end connected to an output terminal of the operational amplifier;

[0037] a first control switch having one end connected to the internal data line, and an other end connected to the output terminal of the operational amplifier; and

[0038] a second control switch having one end connected to the data signal line, and an other end connected to the internal data line,

[0039] the AD conversion circuit is provided per plurality of the output and current-monitoring circuits,

[0040] when a row for which the characteristic detection process is performed during a frame period is defined as a monitored row, and a row other than the monitored row is defined as a non-monitored row, the frame period includes a characteristic detection processing period including: a detection preparation period during which preparation for detecting a characteristic of the characteristic detection target circuit element is performed in the monitored row; a current measurement period during which a characteristic of the characteristic detection target circuit element is detected by measuring a current flowing through the data signal line; and a light emission preparation period during which preparation for allowing the electrooptical element to emit light is performed in the monitored row,

[0041] the current measurement period includes: a data signal line charging period during which the data signal line is charged such that a current of a magnitude according to the characteristic of the characteristic detection target circuit element flows through the data signal line; a monitoring period during which the monitored data is obtained by accumulating a time-integrated value of the current flowing through the data signal line in the second capacitor; and an AD conversion period during which the AD conversion circuit converts the monitored data from the analog value to the digital value, and

[0042] during the AD conversion period,

[0043] the data signal line and the internal data line are electrically disconnected from each other by bringing the second control switch into an off state, and

[0044] the AD conversion circuit sequentially converts the plurality of pieces of monitored data from analog values to digital values, the plurality of pieces of monitored data being obtained by a plurality of corresponding output and current-monitoring circuits.

[0045] According to a second aspect of the present invention, in the first aspect of the present invention,

[0046] the current measurement period includes: a drive transistor characteristic detection period during which current measurement for detecting a characteristic of the drive transistor is performed; and an electrooptical element characteristic detection period during which current measurement for detecting a characteristic of the electrooptical element is performed.

[0047] According to a third aspect of the present invention, in the second aspect of the present invention,

[0048] the output and current-monitoring circuit further includes a third control switch having one end connected to the data signal line, and an other end connected to a predetermined control line, and

[0049] in the drive transistor characteristic detection period included in the current measurement period, during the AD conversion period, the data signal line and the control line are electrically connected to each other by bringing the third control switch into an on state, and a potential of a magnitude is provided to the control line, the magnitude being equal to a magnitude of a potential provided to the data signal line during the data signal line charging period.

[0050] According to a fourth aspect of the present invention, in the third aspect of the present invention,

[0051] in the electrooptical element characteristic detection period included in the current measurement period, during the AD conversion period, the third control switch is brought into an off state and the monitoring control transistor is brought into an off state, so that the data signal line goes into a high-impedance state.

[0052] According to a fifth aspect of the present invention, in the third aspect of the present invention,

[0053] in the electrooptical element characteristic detection period included in the current measurement period, during the AD conversion period, the data signal line and the control line are electrically connected to each other by bringing the third control switch into an on state, and a potential of a magnitude is provided to the control line, the magnitude being substantially equal to a magnitude of a potential provided to the data signal line during the data signal line charging period.

[0054] According to a sixth aspect of the present invention, in the third aspect of the present invention,

[0055] in the electrooptical element characteristic detection period included in the current measurement period, during the AD conversion period, the data signal line and the control line are electrically connected to each other by bringing the third control switch into an on state, and a potential of certain magnitude is provided to the control line, the potential of certain magnitude being close to a potential to be provided to the data signal line during the data signal line charging period.

[0056] According to a seventh aspect of the present invention, in the second aspect of the present invention,

[0057] when a potential provided to the data signal line during the detection preparation period is Vmg, a potential provided to the data signal line during the drive transistor characteristic detection period is Vm_TFT, and a potential provided to the data signal line during the electrooptical element characteristic detection period is Vm_oled, values of Vmg, Vm_TFT, and Vm_oled are set so as to satisfy following relationships:

[0058] $Vm\_TFT<Vmg-Vth(T2)$

[0059] $Vm\_TFT<ELVSS+Vth(oled)$

[0060] Vm_oled>Vmg−Vth(T2)

[0061] Vm_oled>ELVSS+Vth(oled)

[0062] where Vth(T2) is a threshold voltage of the drive transistor, Vth(oled) is a light emission threshold voltage of the electrooptical element, and ELVSS is a cathode potential of the electrooptical element.

[0063] According to an eighth aspect of the present invention, in the first aspect of the present invention,

[0064] the characteristic detection processing period is provided in a vertical retrace period.

[0065] According to a ninth aspect of the present invention, in the eighth aspect of the present invention,

[0066] with any electrooptical element defined as a focused electrooptical element, when the focused electrooptical element is included in the monitored row, the pixel circuit driving unit provides to the data signal line a potential of a data signal corresponding to a larger grayscale voltage than a grayscale voltage provided when the focused electrooptical element is included in the non-monitored row, upon performing writing of the data signal to a pixel circuit included in the monitored row during a vertical scanning period.

[0067] According to a tenth aspect of the present invention, in the first aspect of the present invention,

[0068] the characteristic detection processing period is provided in a vertical scanning period.

[0069] According to an eleventh aspect of the present invention, in the first aspect of the present invention,

[0070] a cycle is repeated a plurality of times during a current measurement period for detecting a characteristic of one characteristic detection target circuit element, the cycle including the data signal line charging period, the monitoring period, and the AD conversion period.

[0071] According to a twelfth aspect of the present invention, in the first aspect of the present invention,

[0072] the characteristic detection process for only either one of the electrooptical element and the drive transistor is performed per frame period.

[0073] A thirteenth aspect of the present invention is directed to a method for driving a display device including: a pixel matrix of n rows×m columns including n×m pixel circuits (n and m are integers greater than or equal to 2), each pixel circuit including an electrooptical element whose luminance is controlled by a current and a drive transistor for controlling a current to be supplied to the electrooptical element; scanning lines provided for the respective rows of the pixel matrix; monitoring control lines provided for the respective rows of the pixel matrix; data signal lines provided for the respective columns of the pixel matrix; and a pixel circuit driving unit configured to drive the scanning lines, the monitoring control lines, and the data signal lines, the method including:

[0074] a characteristic detecting step of detecting, during a frame period, a characteristic of a characteristic detection target circuit element including at least one of the electrooptical element and the drive transistor;

[0075] a correction data storing step of allowing a correction data storage unit to store characteristic data obtained based on results of the detection in the characteristic detecting step, as correction data for correcting video signals, the correction data storage unit being prepared in advance; and a video signal correcting step of generating data signals to be supplied to the n×m pixel circuits by correcting the video signals based on the correction data stored in the correction data storage unit, wherein

[0076] each of the pixel circuits includes:

[0077] the electrooptical element;

[0078] an input transistor having a control terminal connected to the scanning line, a first conduction terminal connected to a control terminal of the drive transistor, and a second conduction terminal connected to the data signal line;

[0079] the drive transistor having a first conduction terminal to which a drive power supply potential is provided;

[0080] a monitoring control transistor having a control terminal connected to the monitoring control line, a first conduction terminal connected to a second conduction terminal of the drive transistor and an anode of the electrooptical element, and a second conduction terminal connected to the data signal line; and

[0081] a first capacitor having one end connected to the control terminal of the drive transistor to hold a potential of the control terminal of the drive transistor,

[0082] the pixel circuit driving unit includes:

[0083] an output and current-monitoring circuit having a function of applying the data signal to the data signal line and a function of obtaining, as monitored data, data according to a magnitude of a current flowing through the data signal line, the monitored data being base data for the characteristic data; and

[0084] an AD conversion circuit configured to convert the monitored data from an analog value to a digital value,

[0085] the output and current-monitoring circuit includes:

[0086] an internal data line connected to the data signal line;

[0087] an operational amplifier having a non-inverting input terminal to which the data signal is provided, and an inverting input terminal connected to the internal data line;

[0088] a second capacitor having one end connected to the internal data line, and an other end connected to an output terminal of the operational amplifier;

[0089] a first control switch having one end connected to the internal data line, and an other end connected to the output terminal of the operational amplifier; and

[0090] a second control switch having one end connected to the data signal line, and an other end connected to the internal data line,

[0091] the AD conversion circuit is provided per plurality of the output and current-monitoring circuits,

[0092] when a row for which the characteristic detection process is performed during a frame period is defined as a monitored row, and a row other than the monitored row is defined as a non-monitored row,

[0093] the characteristic detecting step includes:

[0094] a detection preparing step of preparing for detecting a characteristic of the characteristic detection target circuit element in the monitored row;

[0095] a current measuring step of detecting a characteristic of the characteristic detection target circuit element by measuring a current flowing through the data signal line; and

[0096] a light emission preparing step of preparing for allowing the electrooptical element to emit light in the monitored row,

[0097] the current measuring step includes:

[0098] a data signal line charging step of charging the data signal line such that a current of a magnitude according to the characteristic of the characteristic detection target circuit element flows through the data signal line;

[0099] a monitoring step of obtaining monitored data by accumulating a time-integrated value of the current flowing through the data signal line in the second capacitor; and

[0100] an AD converting step of converting, by the AD conversion circuit, the monitored data from the analog value to the digital value, and

[0101] in the AD converting step,

[0102] the data signal line and the internal data line are electrically disconnected from each other by bringing the second control switch into an off state, and

[0103] the AD conversion circuit sequentially converts the plurality of pieces of monitored data from analog values to digital values, the plurality of pieces of monitored data being obtained by a plurality of corresponding output and current-monitoring circuits.

Effects of the Invention

[0104] According to the first aspect of the present invention, in a display device having pixel circuits, each including an electrooptical element (e.g., an organic EL element) whose luminance is controlled by a current, and a drive transistor for controlling a current to be supplied to the electrooptical element, detection of a characteristic of a circuit element (at least one of the electrooptical element and the drive transistor) is performed during a frame period. Then, a video signal is corrected using correction data which is obtained taking into account a result of the detection. Since a data signal generated based on the thus corrected video signal is supplied to the pixel circuit, a drive current of a magnitude that compensates for degradation of the circuit element is supplied to the electrooptical element. Here, the characteristic of the circuit element is detected by measuring a current flowing through a data signal line. That is, the data signal line is not only used as a signal line that transfers a signal for allowing an electrooptical element in each pixel circuit to emit light at a desired luminance, but also used as a signal line for characteristic detection. Hence, new signal lines do not need to be provided in the display unit to detect characteristics of circuit elements. Accordingly, it becomes possible to compensate for degradation of the circuit elements while an increase in circuit size is suppressed.

[0105] In addition, during an AD conversion period, by a second switch going into an off state, analog data obtained during a monitoring period is held in an output and current-monitoring circuit. Using this function of holding analog data (sample and hold function), an AD conversion circuit is shared between a plurality of columns. This effectively suppresses an increase in circuit size associated with implementation of a configuration capable of detecting characteristics of the circuit elements.

[0106] According to the second aspect of the present invention, detection of characteristics of an electrooptical element and a drive transistor is performed during a frame period. Hence, it becomes possible to compensate for both of degradation of the electrooptical element and degradation of the drive transistor while an increase in circuit size is effectively suppressed.

[0107] According to the third aspect of the present invention, during an AD conversion period included in a drive transistor characteristic detection period, a data signal line and an internal data line are electrically disconnected from each other, and a potential of a magnitude equal to a potential of the data signal line that is obtained immediately before the AD conversion period is provided to the data signal line from a control line. Hence, the potential of the data signal line is prevented from being changed during AD conversion due to sharing of an AD conversion circuit. In addition, since recharging of the data signal line is performed in a very short period of time, it becomes possible to repeatedly perform current measurement for characteristic detection. By this, it becomes possible to ensure a sufficient S/N ratio upon current measurement for detecting a characteristic of a drive transistor.

[0108] According to the fourth aspect of the present invention, during an AD conversion period included in an electrooptical element characteristic detection period, a data signal line is brought into a high-impedance state. Hence, the potential of the data signal line is prevented from being changed during AD conversion due to sharing of an AD conversion circuit. In addition, since recharging of the data signal line is performed in a very short period of time, it becomes possible to repeatedly perform current measurement for characteristic detection. By this, it becomes possible to ensure a sufficient S/N ratio upon current measurement for detecting a characteristic of an electrooptical element.

[0109] According to the fifth aspect of the present invention, during an AD conversion period included in an electrooptical element characteristic detection period, a data signal line and an internal data line are electrically disconnected from each other, and a potential of a magnitude equal to a potential of the data signal line that is obtained immediately before the AD conversion period is provided to the data signal line from a control line. Hence, the potential of the data signal line is prevented from being changed during AD conversion due to sharing of an AD conversion circuit. In addition, since recharging of the data signal line is performed in a very short period of time, it becomes possible to repeatedly perform current measurement for characteristic detection. By this, it becomes possible to ensure a sufficient S/N ratio upon current measurement for detecting a characteristic of an electrooptical element.

[0110] According to the sixth aspect of the present invention, as with the fifth aspect of the present invention, it becomes possible to ensure a sufficient S/N ratio upon current measurement for detecting a characteristic of an electrooptical element.

[0111] According to the seventh aspect of the present invention, during a drive transistor characteristic detection period, a drive transistor securely goes into an on state and an electrooptical element securely goes into an off state. In addition, during an electrooptical element characteristic detection period, the drive transistor securely goes into an off state and the electrooptical element securely goes into an on state.

[0112] According to the eighth aspect of the present invention, for a monitored row, after performing writing during a

vertical scanning period, writing is performed again during a light emission preparation period included in a vertical retrace period. In this regard, in order to enable writing during the light emission preparation period, corresponding data needs to be held after performing writing during the vertical scanning period. Regarding this point, since the data to be held is merely data for one line, an increase in memory capacity is a little. On the other hand, in a configuration in which a characteristic detection processing period is provided in a vertical scanning period, a line memory for several tens of lines may be required. By the above, required memory capacity is reduced compared to the configuration in which a characteristic detection processing period is provided in a vertical scanning period.

[0113] According to the ninth aspect of the present invention, a potential of a data signal is adjusted taking into account the fact that in a monitored row an electrooptical element is temporarily turned off during a vertical retrace period. Hence, a degradation in display quality is suppressed.

[0114] According to the tenth aspect of the present invention, unlike a configuration in which a characteristic detection processing period is provided in a vertical retrace period, writing according to a target luminance in a monitored row needs to be performed only once in one frame period.

[0115] According to the eleventh aspect of the present invention, current measurement is repeated a plurality of times during each current measurement period for detecting a characteristic of a characteristic detection target circuit element. Hence, a sufficient S/N ratio can be ensured.

[0116] According to the twelfth aspect of the present invention, by performing a characteristic detection process for only either one of an electrooptical element and a drive transistor per frame period, sufficient time for transferring data obtained by AD conversion is ensured after the AD conversion.

[0117] According to the thirteenth aspect of the present invention, the same effects as those of the first aspect of the present invention can be provided by an invention of a method for driving a display device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0118] FIG. **1** is a circuit diagram showing detailed configurations of a pixel circuit, an output and current-monitoring circuit, and a signal conversion circuit in one embodiment of the present invention.

[0119] FIG. **2** is a block diagram showing an overall configuration of an active matrix-type organic EL display device according to the embodiment.

[0120] FIG. **3** is a timing chart for describing the operation of a gate driver in the embodiment.

[0121] FIG. **4** is a timing chart for describing the operation of the gate driver in the embodiment.

[0122] FIG. **5** is a timing chart for describing the operation of the gate driver in the embodiment.

[0123] FIG. **6** is a diagram for describing input and output signals of an output and current-monitoring circuit in an output unit in the embodiment.

[0124] FIG. **7** is a diagram for describing adjustment of the length of integral time by control of a control clock signal CLK**1** in the embodiment.

[0125] FIG. **8** is a diagram for describing sharing of A/D converts in the embodiment.

[0126] FIG. **9** is a diagram for describing a transition of operation for each row in the embodiment.

[0127] FIG. **10** is a timing chart for describing the operation of a pixel circuit (a pixel circuit at an ith row and a jth column) included in a monitored row in the embodiment.

[0128] FIG. **11** is a diagram for describing the flow of a current for when normal operation is performed in the embodiment.

[0129] FIG. **12** is a timing chart for describing details of one horizontal scanning period for a monitored row in the embodiment.

[0130] FIG. **13** is a diagram for describing the flow of a current during a detection preparation period in the embodiment.

[0131] FIG. **14** is a diagram for describing the flow of a current during a period Tb**2** included in a TFT characteristic detection period in the embodiment.

[0132] FIG. **15** is a diagram for describing a state of a circuit during a period Tb**3** included in the TFT characteristic detection period in the embodiment.

[0133] FIG. **16** is a diagram for describing the flow of a current during a period Tc**2** included in an OLED characteristic detection period in the embodiment.

[0134] FIG. **17** is a diagram for describing the flow of a current during a light emission preparation period in the embodiment.

[0135] FIG. **18** is a diagram for describing the flow of a current during a light emission period in the embodiment.

[0136] FIG. **19** is a diagram comparing one frame period for a monitored row with one frame period for a non-monitored row in the embodiment.

[0137] FIG. **20** is a flowchart for describing a procedure for updating correction data in a correction data storage unit in the embodiment.

[0138] FIG. **21** is a diagram for describing correction of a video signal in the embodiment.

[0139] FIG. **22** is a flowchart for describing an outline of operation related to detection of a TFT characteristic and an OLED characteristic in the embodiment.

[0140] FIG. **23** is a diagram for describing an effect of the embodiment.

[0141] FIG. **24** is a diagram for describing an effect of the embodiment.

[0142] FIG. **25** is a timing chart for describing the operation of a pixel circuit (a pixel circuit at an ith row and a jth column) included in a monitored row in a second variant of the embodiment.

[0143] FIG. **26** is a timing chart for describing details of one horizontal scanning period for a monitored row in the second variant of the embodiment.

[0144] FIG. **27** is a circuit diagram showing a configuration in which a control line CL and a switch **335** are removed from the configuration shown in FIG. **1**, in the second variant of the embodiment.

[0145] FIG. **28** is a diagram for describing a configuration of one frame period.

[0146] FIG. **29** is a timing chart for describing the operation, during a vertical retrace period, of a pixel circuit (assumed to be a pixel circuit at an ith row and a jth column) included in a monitored row in a third variant of the embodiment.

[0147] FIG. **30** is a timing chart for describing details of the vertical retrace period in the third variant of the embodiment.

[0148] FIG. **31** is a timing chart for describing the operation, during one frame period, of a pixel circuit (assumed to be a pixel circuit at an ith row and a jth column) included in a monitored row in the third variant of the embodiment.

[0149] FIG. **32** is a circuit diagram showing a configuration of a conventional common pixel circuit.

[0150] FIG. **33** is a timing chart for describing the operation of the pixel circuit shown in FIG. **32**.

[0151] FIG. **34** is a diagram for describing a case in which no compensation is performed for degradation of a drive transistor and degradation of an organic EL element.

[0152] FIG. **35** is a diagram for describing a case in which compensation is performed only for degradation of a drive transistor.

[0153] FIG. **36** is FIG. 14 of Published Japanese Translation of PCT Application No. 2008-523448.

MODE FOR CARRYING OUT THE INVENTION

[0154] One embodiment of the present invention will be described below with reference to the accompanying drawings. Note that in the following it is assumed that m and n are integers greater than or equal to 2, i is an integer between 1 and n, inclusive, and j is an integer between 1 and m, inclusive. Note also that in the following a characteristic of a drive transistor provided in a pixel circuit is referred to as "TFT characteristic" and a characteristic of an organic EL element provided in the pixel circuit is referred to as "OLED characteristic".

[0155] <1. Overall Configuration>

[0156] FIG. **2** is a block diagram showing an overall configuration of an active matrix-type organic EL display device **1** according to one embodiment of the present invention. The organic EL display device **1** includes a display unit **10**, a control circuit **20**, a source driver (data signal line drive circuit) **30**, a gate driver (scanning line drive circuit) **40**, and a correction data storage unit **50**. In the present embodiment, a pixel circuit driving unit is implemented by the source driver **30** and the gate driver **40**. Note that the configuration may be such that one or both of the source driver **30** and the gate driver **40** are integrally formed with the display unit **10**.

[0157] In the display unit **10** there are disposed m data signal lines S(**1**) to S(m) and n scanning lines G**1**(**1**) to G**1**(n) which intersect the m data signal lines S(**1**) to S(m). In the following, an extension direction of the data signal lines is a Y-direction and an extension direction of the scanning lines is an X-direction. Components lying along the Y-direction may be referred to as "column" and components lying along the X-direction may be referred to as "row". In addition, in the display unit **10**, n monitoring control lines G**2**(**1**) to G**2**(n) are disposed so as to have a one-to-one correspondence with the n scanning lines G**1**(**1**) to G**1**(n). The scanning lines G**1**(**1**) to G**1**(n) and the monitoring control lines G**2**(**1**) to G**2**(n) are parallel to each other. Furthermore, in the display unit **10**, n×m pixel circuits **11** are provided at the respective intersections of the n scanning lines G**1**(**1**) to G**1**(n) and the m data signal lines S(**1**) to S(m). By thus providing the n×m pixel circuits **11**, a pixel matrix of n rows×m columns is formed in the display unit **10**. In addition, there are disposed high-level power supply lines that supply a high-level power supply voltage and low-level power supply lines that supply a low-level power supply voltage in the display unit **10**.

[0158] Note that in the following, when the m data signal lines S(**1**) to S(m) do not need to be distinguished from each other, the data signal line is simply represented by reference character S. Likewise, when the n scanning lines G**1**(**1**) to G**1** (n) do not need to be distinguished from each other, the scanning line is simply represented by reference character G**1**, and when the n monitoring control lines G**2**(**1**) to G**2**(n) do not need to be distinguished from each other, the monitoring control line is simply represented by reference character G**2**.

[0159] The data signal line S in the present embodiment is not only used as a signal line that transfers a luminance signal for allowing an organic EL element in a pixel circuit **11** to emit light at a desired luminance, but also used as a signal line for providing control potentials for detecting a TFT characteristic and an OLED characteristic to the pixel circuit **11**, and as a signal line serving as a path for currents that represent a TFT characteristic and an OLED characteristic and that are measurable by an output and current-monitoring circuit **330** which will be described later.

[0160] The control circuit **20** controls the operation of the source driver **30** by providing data signals DA and a source control signal SCTL to the source driver **30**, and controls the operation of the gate driver **40** by providing a gate control signal GCTL to the gate driver **40**. The source control signal SCTL includes, control clock signals CLK**1**, CLK**2**, and CLK**2**B for controlling the operation of the output and current-monitoring circuits **330**, in addition to a source start pulse, a source clock, and a latch strobe signal which are used conventionally, for example. The gate control signal GCTL includes, for example, a gate start pulse, a gate clock, and an output enable signal. In addition, the control circuit **20** receives monitored data MO which is provided from the source driver **30**, and performs an update to correction data stored in the correction data storage unit **50**. Note that the monitored data MO is data measured to obtain a TFT characteristic and an OLED characteristic.

[0161] The gate driver **40** is connected to the n scanning lines G**1**(**1**) to G**1**(n) and the n monitoring control lines G**2**(**1**) to G**2**(*n*). The gate driver **40** is composed of a shift register, a logic circuit, and the like. Meanwhile, in the organic EL display device **1** according to the present embodiment, a video signal (base data for the above-described data signal DA) which is transmitted from an external source is corrected based on a TFT characteristic and an OLED characteristic. In this regard, in the present embodiment, in each frame, detection of a TFT characteristic and an OLED characteristic for one row is performed. Specifically, when detection of a TFT characteristic and an OLED characteristic for the first row is performed in a given frame, detection of a TFT characteristic and an OLED characteristic for the second row is performed in the next frame, and detection of a TFT characteristic and an OLED characteristic for the third row is performed in the frame after the next frame. In this manner, detection of a TFT characteristic and an OLED characteristic for n rows is performed over n frame periods. Note that in this specification a row for which detection of a TFT characteristic and an OLED characteristic is performed when focusing on any frame is referred to as "monitored row", and a row other than the monitored row is referred to as "non-monitored row".

[0162] Here, when a frame in which detection of a TFT characteristic and an OLED characteristic for the first row is performed is defined as a (k+1)th frame, in the (k+1)th frame

the n scanning lines G1(1) to G1(n) and the n monitoring control lines G2(1) to G2(n) are driven in a manner shown in FIG. **3**, in a (k+2)th frame the n scanning lines G1(1) to G1 (n) and the n monitoring control lines G2(1) to G2(n) are driven in a manner shown in FIG. **4**, and in a (k+n)th frame the n scanning lines G1(1) to G1(n) and the n monitoring control lines G2(1) to G2(n) are driven in a manner shown in FIG. **5**. Note that for FIGS. **3** to **5** a high-level state is an active state. Note also that in FIGS. **3** to **5** one horizontal scanning period for a monitored row is represented by reference character THm, and one horizontal scanning period for a non-monitored row is represented by reference character THn.

[0163] As can be grasped from FIGS. **3** to **5**, the length of one horizontal scanning period is different between the monitored row and the non-monitored row. Specifically, the length of one horizontal scanning period for the monitored row is longer than that of one horizontal scanning period for the non-monitored row. For the non-monitored row, one frame period includes one selection period as with a common organic EL display device. For the monitored row, unlike a common organic EL display device, one frame period includes two selection periods. Note that a more detailed description of one horizontal scanning period THm for the monitored row will be made later.

[0164] As shown in FIGS. **3** to **5**, in each frame, monitoring control lines G2 corresponding to a non-monitored row are maintained in a non-active state. A monitoring control line G2 corresponding to a monitored row is maintained in an active state during a period other than selection periods in one horizontal scanning period THm (a period during which a scanning line G1 is in a non-active state). In the present embodiment, the gate driver **40** is configured such that the n scanning lines G1(1) to G1(n) and the n monitoring control lines G2(1) to G2(n) are driven in the above-described manner. Note that to generate two pulses on a scanning line G1 during one frame period in a monitored row, the waveform of an output enable signal which is transmitted to the gate driver **40** from the control circuit **20** may be controlled using publicly known techniques.

[0165] The source driver **30** is connected to the m data signal lines S(1) to S(m). The source driver **30** is composed of a drive signal generating circuit **31**, a signal conversion circuit **32**, and an output unit **33** including m output and current-monitoring circuits **330** (see FIG. **2**). Each of the m output and current-monitoring circuits **330** in the output unit **33** is connected to their corresponding data signal line S among the m data signal lines S(1) to S(m).

[0166] The drive signal generating circuit **31** includes a shift register, a sampling circuit, and a latch circuit. In the drive signal generating circuit **31**, the shift register sequentially transfers a source start pulse from an input terminal to an output terminal in synchronization with a source clock. According to the transfer of the source start pulse, sampling pulses for the respective data signal lines S are outputted from the shift register. The sampling circuit sequentially stores data signals DA for one row, according to timing of the sampling pulses. The latch circuit catches the data signals DA for one row which are stored in the sampling circuit, according to a latch strobe signal, and holds the data signals DA.

[0167] Note that in the present embodiment data signal DA includes a luminance signal for allowing an organic EL element in each pixel to emit light at a desired luminance, and a monitoring control signal for controlling the operation of the pixel circuit **11** when detecting a TFT characteristic and an OLED characteristic.

[0168] The signal conversion circuit **32** includes a D/A converter and an A/D converter. The data signals DA for one row which are held in the latch circuit in the drive signal generating circuit **31** in the above-described manner are converted into analog voltages by the D/A converter in the signal conversion circuit **32**. The converted analog voltages are provided to the output and current-monitoring circuits **330** in the output unit **33**. In addition, monitored data MO is provided to the signal conversion circuit **32** from the output and current-monitoring circuits **330** in the output unit **33**. The monitored data MO is converted from an analog voltage into a digital signal by the A/D converter in the signal conversion circuit **32**. Then, the monitored data MO converted into the digital signal is provided to the control circuit **20** through the drive signal generating circuit **31**.

[0169] FIG. **6** is a diagram for describing input and output signals of an output and current-monitoring circuit **330** in the output unit **33**. An analog voltage Vs serving as a data signal DA is provided to the output and current-monitoring circuit **330** from the signal conversion circuit **32**. The analog voltage Vs is applied to a data signal line S through a buffer in the output and current-monitoring circuit **330**. In addition, the output and current-monitoring circuit **330** has a function of obtaining a magnitude of a current flowing through the data signal line S, as analog data (analog voltage), and a function of holding the value of analog data obtained at given timing, throughout a period during which AD conversion is performed (i.e., a sample and hold function). The data obtained by the output and current-monitoring circuit **330** is provided as monitored data MO to the signal conversion circuit **32**. Note that a detailed configuration of the output and current-monitoring circuit **330** will be described later (see FIG. **1**).

[0170] The correction data storage unit **50** includes a TFT offset memory **51***a*, an OLED offset memory **51***b*, a TFT gain memory **52***a*, and an OLED gain memory **52***b* (see FIG. **2**). Note that these four memories may be physically one memory or may be physically different memories. The correction data storage unit **50** stores therein correction data which is used to correct video signals transmitted from an external source. Specifically, the TFT offset memory **51***a* stores, as correction data, an offset value obtained based on a result of detection of a TFT characteristic. The OLED offset memory **51***b* stores, as correction data, an offset value obtained based on a result of detection of an OLED characteristic. The TFT gain memory **52***a* stores, as correction data, a gain value obtained based on the result of detection of a TFT characteristic. The OLED gain memory **52***b* stores, as correction data, a degradation correction factor obtained based on the result of detection of an OLED characteristic. Note that typically offset values and gain values whose numbers are equal to the number of pixels in the display unit **10** are stored in the TFT offset memory **51***a* and the TFT gain memory **52***a*, respectively, as correction data based on results of detection of a TFT characteristic. Note also that typically offset values and degradation correction factors whose numbers are equal to the number of pixels in the display unit **10** are stored in the OLED offset memory **51***b* and the OLED gain memory **52***b*, respectively, as correction data based on results of detection of an OLED characteristic.

Note, however, that the configuration may be such that each memory stores one value for every plurality of pixels.

[0171] The control circuit **20** updates the offset values in the TFT offset memory **51***a*, the offset values in the OLED offset memory **51***b*, the gain values in the TFT gain memory **52***a*, and the degradation correction factors in the OLED gain memory **52***b*, based on monitored data MO provided from the source driver **30**.

[0172] In addition, the control circuit **20** reads the offset values in the TFT offset memory **51***a*, the offset values in the OLED offset memory **51***b*, the gain values in the TFT gain memory **52***a*, and the degradation correction factors in the OLED gain memory **52***b* to correct video signals. Data obtained by the correction is transmitted as data signals DA to the source driver **30**.

[0173] <2. Detailed Configuration of a Main Part>

[0174] Next, a detailed configuration of a main part of the present embodiment will be described. FIG. **1** is a circuit diagram showing detailed configurations of a pixel circuit **11**, an output and current-monitoring circuit **330**, and a signal conversion circuit **32**. The configurations and operation of these circuits will be described in detail below.

[0175] <2.1 Pixel Circuit>

[0176] The pixel circuit **11** shown in FIG. **1** is a pixel circuit **11** at an ith row and a jth column. The pixel circuit **11** includes one organic EL element OLED, three transistors T**1** to T**3**, and one capacitor Cst. The transistor T**1** functions as an input transistor that selects a pixel, the transistor T**2** functions as a drive transistor that controls the supply of a current to the organic EL element OLED, and the transistor T**3** functions as a monitoring control transistor that controls whether to detect a TFT characteristic and an OLED characteristic. Note that in the present embodiment the transistor T**2** and the organic EL element OLED correspond to a characteristic detection target circuit element. Note also that for each transistor, a gate terminal corresponds to a control terminal, a drain terminal corresponds to a first conduction terminal, and a source terminal corresponds to a second conduction terminal.

[0177] The transistor T**1** is provided between a data signal line S(j) and the gate terminal of the transistor T**2**. For the transistor T**1**, the gate terminal is connected to a scanning line G**1**(*i*) and the source terminal is connected to the data signal line S(j). The transistor T**2** is provided in series with the organic EL element OLED. For the transistor T**2**, the gate terminal is connected to the drain terminal of the transistor T**1**, the drain terminal is connected to a high-level power supply line ELVDD, and the source terminal is connected to an anode terminal of the organic EL element OLED. For the transistor T**3**, the gate terminal is connected to a monitoring control line G**2**(*i*), the drain terminal is connected to the anode terminal of the organic EL element OLED, and the source terminal is connected to the data signal line S(j). For the capacitor Cst, one end is connected to the gate terminal of the transistor T**2** and the other end is connected to the drain terminal of the transistor T**2**. Note that a first capacitor is implemented by the capacitor Cst. A cathode terminal of the organic EL element OLED is connected to a low-level power supply line ELVSS.

[0178] Meanwhile, in the configuration shown in FIG. **32**, the capacitor Cst is provided between the gate and source of the transistor T**2**. On the other hand, in the present embodiment, the capacitor Cst is provided between the gate and drain of the transistor T**2**. The reason therefor is as follows. Specifically, in the present embodiment, during one frame period, control is performed to change the potential of the data signal line S(j), with the transistor T**3** being in an on state. If the capacitor Cst is provided between the gate and source of the transistor T**2**, the gate potential of the transistor T**2** also changes according to the change in the potential of the data signal line S(j). This may result in the on/off state of the transistor T**2** not going into a desired state. Hence, in the present embodiment, in order that the gate potential of the transistor T**2** does not change according to the change in the potential of the data signal line S(j), the capacitor Cst is provided between the gate and drain of the transistor T**2** as shown in FIG. **1**.

[0179] <2.2 Regarding Transistors in Pixel Circuit>

[0180] In the present embodiment, all of the transistors T**1** to T**3** in the pixel circuit **11** are of the n-channel type. Moreover, in the present embodiment, for the transistors T**1** to T**3**, oxide TFTs (thin film transistors using an oxide semiconductor for channel layers) are adopted.

[0181] A description is made below of an oxide semiconductor layer included in each of the oxide TFTs. The oxide semiconductor layer is, for example, an In—Ga—Zn—O-based semiconductor layer. The oxide semiconductor layer contains, for example, an In—Ga—Zn—O-based semiconductor. The In—Ga—Zn—O-based semiconductor is a ternary oxide of In (indium), Ga (gallium) and Zn (zinc). A ratio (composition ratio) of In, Ga and Zn is not particularly limited. For example, the composition ratio may be In:Ga:Zn=2:2:1, In:Ga:Zn=1:1:1, In:Ga:Zn=1:1:2, and the like.

[0182] Such a TFT including the In—Ga—Zn—O-based semiconductor layer has high mobility (mobility exceeding 20 times that of an amorphous silicon TFT) and a low leak current (leak current of less than 1/100 of that of the amorphous silicon TFT. Accordingly, this TFT is suitably used as a drive TFT (the above-described transistor T**2**) in the pixel circuit and a switching TFT (the above-described transistor T**1**) therein. When the TFT including the In—Ga—Zn—O-based semiconductor layer is used, electric power consumption of the display device can be reduced to a great extent.

[0183] The In—Ga—Zn—O-based semiconductor maybe amorphous, or may include a crystalline portion and have crystallinity. As the crystalline In—Ga—Zn—O-based semiconductor, a crystalline In—Ga—Zn—O-based semiconductor, in which a c-axis is oriented substantially perpendicularly to a layer surface, is preferable. A crystal structure of the In—Ga—Zn—O-based semiconductor as described above is disclosed, for example, in Japanese Patent Application Laid-Open No. 2012-134475.

[0184] The oxide semiconductor layer may contain other oxide semiconductors in place of the In—Ga—Zn—O-based semiconductor. For example, the oxide semiconductor layer may contain a Zn—O-based semiconductor (ZnO), an In—Zn—O-based semiconductor (IZO (registered trademark)), a Zn—Ti—O-based oxide semiconductor (ZTO), a Cd—Ge—O-based semiconductor, a Cd—Pb—O-based semiconductor, a CdO (cadmium oxide), a Mg—Zn—O-based semiconductor, an In—Sn—O-based semiconductor (for example, In_2O_3—SnO_2—ZnO), an In—Ga—Sn—O-based semiconductor and the like.

[0185] <2.3 Output and Current-monitoring Circuit>

[0186] With reference to FIG. **1**, the configuration and operation of the output and current-monitoring circuit **330** of the present embodiment will be described in detail. The output and current-monitoring circuit **330** includes an opera-

tional amplifier **331**, a capacitor **332**, and three switches (switches **333**, **334**, and **335**).

[0187] As shown in FIG. **1**, an internal data line Sin(j) of the output and current-monitoring circuit **330** is connected to the data signal line S(j) through the switch **334**. The operational amplifier **331** has an inverting input terminal connected to the internal data line Sin(j), and a non-inverting input terminal to which an analog voltage Vs serving as a data signal DA is provided. The capacitor **332** and the switch **333** are provided between an output terminal of the operational amplifier **331** and the internal data line Sin(j). A control clock signal CLK**1** is provided to the switch **333**. An integrating circuit is configured by the operational amplifier **331**, the capacitor **332**, and the switch **333**. Now, the operation of the integrating circuit will be described. When the switch **333** is switched from an off state to an on state by the control clock signal CLK**1**, charge accumulated in the capacitor **332** is discharged. When the switch **333** is switched from the on state to the off state thereafter, charging of the capacitor **332** is performed based on a current flowing through the internal data line Sin(j). That is, a time-integrated value of the current flowing through the internal data line Sin(j) is accumulated in the capacitor **332**. By this, the potential of the output terminal of the operational amplifier **331** changes according to the magnitude of the current flowing through the internal data line Sin(j). An output from the operational amplifier **331** is transmitted as monitored data MO to the signal conversion circuit **32**. Note that when the switch **333** is brought into an on state by the control clock signal CLK**1**, a short-circuit state occurs between the output terminal and inverting input terminal of the operational amplifier **331**. By this, the potentials of the output terminal of the operational amplifier **331** and the internal data line Sin(j) become equal to the potential of the analog voltage Vs.

[0188] The switch **334** is provided between the data signal line S(j) and the internal data line Sin(j). A control clock signal CLK**2** is provided to the switch **334**. By switching the state of the switch **334** based on the control clock signal CLK**2**, an electrical connection state between the data signal line S(j) and the internal data line Sin(j) is controlled. In the present embodiment, when the control clock signal CKL**2** is at a high level, the data signal line S(j) and the internal data line Sin(j) go into an electrically connected state, and when the control clock signal CKL**2** is at a low level, the data signal line S(j) and the internal data line Sin(j) go into an electrically disconnected state.

[0189] The switch **335** is provided between the data signal line S(j) and a predetermined control line CL. A control clock signal CLK**2**B is provided to the switch **335**. By switching the state of the switch **335** based on the control clock signal CLK**2**B, an electrical connection state between the data signal line S(j) and the control line CL is controlled. In the present embodiment, when the control clock signal CKL**2**B is at a high level, the data signal line S(j) and the control line CL go into an electrically connected state, and when the control clock signal CKL**2**B is at a low level, the data signal line S(j) and the control line CL go into an electrically disconnected state.

[0190] As described above, when the switch **334** goes into an off state, the data signal line S(j) and the internal data line Sin(j) go into an electrically disconnected state. At this time, if the switch **333** is in an off state, then the potential of the internal data line Sin(j) is maintained. In the present embodiment, with the potential of the internal data line Sin(j) maintained in this manner, AD conversion by the A/D converter **324** in the signal conversion circuit **32** is performed.

[0191] Note that in the present embodiment a first control switch is implemented by the switch **333**, a second control switch is implemented by the switch **334**, and a third control switch is implemented by the switch **335**. Note also that a second capacitor is implemented by the capacitor **332**.

[0192] <2.4 Signal Conversion Circuit>

[0193] With reference to FIG. **1**, the configuration and operation of the signal conversion circuit **32** in the present embodiment will be described in detail. The signal conversion circuit **32** includes a D/A converter **321**, a selector **322**, an offset circuit **323**, and the A/D converter **324**. The D/A converter **321** converts a data signal DA which is a digital signal outputted from the drive signal generating circuit **31**, into an analog voltage Vs. In the present embodiment, the A/D converter **324** is shared between a plurality of columns. To implement this, the selector **322** is provided in the signal conversion circuit **32**. To the selector **322** is provided monitored data MO from a plurality of output and current-monitoring circuits **330**. The selector **322** sequentially outputs the provided plurality of pieces of monitored data MO in a time-division manner. The offset circuit **323** has a function of setting the same input level to the A/D converter **324** between when a TFT characteristic is detected and when an OLED characteristic is detected (offset adjustment function). The reason that the offset circuit **323** is provided is that Vm_TFT which is a reference potential for when a TFT characteristic is detected and Vm_oled which is a reference potential for when an OLED characteristic is detected are different potentials. The A/D converter **324** converts an analog voltage outputted from the offset circuit **323** into a digital signal. Note that an offset value used for offset adjustment may be allowed to depend on the value of Vm_TFT and the value of Vm_oled. By the above, for the components in the signal conversion circuit **32**, one D/A converter **321** is provided for each column, and one selector **322**, one offset circuit **323**, and one A/D converter **324** are provided for a plurality of columns.

[0194] Now, a more detailed description will be made of an influence exerted on AD conversion due to the fact that Vm_TFT and Vm_oled have different magnitudes, and how to deal with the influence. Since Vm_TFT and Vm_oled are potentials of different magnitudes, if the offset circuit **323** is not provided, then an input DC level to the A/D converter **324** changes between when a TFT characteristic is detected and when an OLED characteristic is detected. Due to this, the resolution of AD conversion by the A/D converter **324** is wasted (not effectively used). Hence, in the present embodiment, the above-described offset circuit **323** is provided. The offset circuit **323** adjusts the input DC level to the A/D converter **324** by Voffset**1** when a TFT characteristic is detected and by Voffset**2** when an OLED characteristic is detected. By this, it becomes possible to make the DC level for AD conversion performed by the A/D converter **324** substantially constant, and thus, the resolution of AD conversion is effectively used. Note that although here a description is made of an example case in which there are two types of offset levels, the present invention is not limited thereto. For example, when the value of Vm_oled is different between R, G, and B, the configuration may be such that three types of offset levels are prepared for when an OLED

characteristic is detected, and the offset levels are used in a switching manner. In addition, depending on a current measurement condition, a predicted value of a measured current may be large at one time and small at another time. In this regard, by controlling the control clock signal CLK**1** provided to the switch **333** in a manner shown in, for example, FIG. **7** to change the length of integral time (the off time of the control clock signal CLK**1**), too, it becomes possible to effectively use the resolution of AD conversion by the A/D converter **324**. By this, even when a measured current is small, it becomes possible to ensure a sufficient S/N ratio.

[0195] <2.5 Sharing of the A/D Converter>

[0196] As described above, in the present embodiment, the A/D converter **324** is shared between a plurality of columns. This will be described in detail with reference to FIG. **8**. Note that FIG. **8** shows an example of a case in which the source driver **30** has an output unit **33** with **1440** channels (i.e., a case in which **1440** data signal lines S are provided). In the example shown in FIG. **8**, one A/D converter **324** is shared between **144** columns. Therefore, one selector **322** is provided for every **144** columns. To each selector **322** is provided monitored data MO from **144** output and current-monitoring circuits **330**. Then, each selector **322** sequentially provides the **144** pieces of monitored data MO to an offset circuit **323** in a time-division manner. The pieces of monitored data MO provided to the offset circuit **323** are adjusted for their input levels and then provided to the A/D converter **324**. Meanwhile, as described above, by the above-described sample and hold function, the output and current-monitoring circuit **330** holds the value of analog data throughout a period during which AD conversion is performed. By this, the values of analog data obtained at the same timing for all columns are sequentially provided to the A/D converter **324**. Note that the AD-converted monitored data MO is transmitted to the control circuit **20** through a logic unit **311** in the drive signal generating circuit **31**.

[0197] Although in the above-described example one A/D converter **324** is shared between **144** columns, the present invention is not limited thereto. The number of columns sharing one A/D converter **324** may be determined according to the ability of the A/D converter **324**, i.e., the sampling frequency of the A/D converter **324**. The number of columns sharing one A/D converter **324** can be increased as the sampling frequency of the A/D converter **324** increases.

[0198] <3. Drive Method>

[0199] <3.1 Summary>

[0200] Next, a drive method of the present embodiment will be described. As described above, in the present embodiment, detection of a TFT characteristic and an OLED characteristic for one row is performed in each frame. In each frame, operation (hereinafter, referred to as "characteristic detection operation") is performed to detect a TFT characteristic and an OLED characteristic for a monitored row, and normal operation is performed for a non-monitored row. Specifically, when a frame in which detection of a TFT characteristic and an OLED characteristic for the first row is performed is defined as a (k+1)th frame, operation for each row transitions as shown in FIG. **9**. In addition, when detection of a TFT characteristic and an OLED characteristic is performed, an update to correction data in the correction data storage unit **50** is performed using results of the detection. Then, correction of the video signal is performed using the correction data stored in the correction data storage unit **50**.

[0201] FIG. **10** is a timing chart for describing the operation of a pixel circuit **11** (assumed to be a pixel circuit **11** at an ith row and a jth column) included in a monitored row. Note that in FIG. **10** "one frame period" is represented with reference to the first selection period start time point of the ith row in a frame in which the ith row is a monitored row. Note also that here a period included in one frame period other than one horizontal scanning period THm for a monitored row is referred to as "light emission period". The light emission period is denoted by reference character TL. As shown in FIG. **10**, one horizontal scanning period THm for the monitored row includes a period Ta during which preparation for detecting a TFT characteristic and an OLED characteristic is performed in the monitored row (hereinafter, referred to as "detection preparation period"); a period Tb during which current measurement for detecting a TFT characteristic is performed (hereinafter, referred to as "TFT characteristic detection period"); a period Tc during which current measurement for detecting an OLED characteristic is performed (hereinafter, referred to as "OLED characteristic detection period"); and a period Td during which preparation for allowing an organic EL element OLED to emit light is performed in the monitored row (hereinafter, referred to as "light emission preparation period"). Note that in the present embodiment a current measurement period is implemented by the TFT characteristic detection period Tb and the OLED characteristic detection period Tc.

[0202] During the detection preparation period Ta, the scanning line G**1**(*i*) is brought into an active state, the monitoring control line G**2**(*i*) is brought into a non-active state, and a potential Vmg is provided to the data signal line S(j). During the TFT characteristic detection period Tb, the scanning line G**1**(*i*) is brought into a non-active state, the monitoring control line G**2**(*i*) is brought into an active state, and a potential Vm_TFT is provided to the data signal line S(j). During the OLED characteristic detection period Tc, the scanning line G**1**(*i*) is brought into a non-active state, the monitoring control line G**2**(*i*) is brought into an active state, and a potential Vm_oled is provided to the data signal line S(j). During the light emission preparation period Td, the scanning line G**1**(*i*) is brought into an active state, the monitoring control line G**2**(*i*) is brought into a non-active state, and a data potential D(i, j) according to a target luminance of the organic EL element OLED included in the monitored row is provided to the data signal line S(j). During the light emission period TL, the scanning line G**1**(*i*) and the monitoring control line G**2**(*i*) are brought into a non-active state. In addition, during the TFT characteristic detection period Tb, the potential Vm_TFT is provided to the control line CL, for example, from a power supply circuit, and during the OLED characteristic detection period Tc, the potential Vm_oled is provided to the control line CL, for example, from the power supply circuit. Note that a detailed description of the potential Vmg, the potential Vm_TFT, and the potential Vm_oled will be made later.

[0203] <3.2 Operation of the Pixel Circuit>

[0204] <3.2.1 Normal Operation>

[0205] In each frame, for a non-monitored row, normal operation is performed. In the pixel circuit **11** included in the non-monitored row, writing based on a data potential Vdata corresponding to a target luminance is performed during a

selection period, and then the transistor T1 is maintained in an off state. By the writing based on the data potential Vdata, the transistor T2 goes into an on state. The transistor T3 is maintained in an off state. By the above, a drive current is supplied to the organic EL element OLED through the transistor T2, as indicated by an arrow denoted by reference character **71** in FIG. **11**. By this, the organic EL element OLED emits light at a luminance according to the drive current.

[0206] <3.2.2 Characteristic Detection Operation>

[0207] In each frame, for a monitored row, characteristic detection operation is performed. FIG. **12** is a timing chart for describing details of one horizontal scanning period THm for a monitored row. Note that a characteristic detection processing period is implemented by the one horizontal scanning period THm. As shown in FIG. **12**, in the present embodiment, a TFT characteristic detection period Tb is composed of periods Tb**1** to Tb**6**, and an OLED characteristic detection period Tc is composed of periods Tc**1** to Tc**6**. Note that in the present embodiment a data signal line charging period is implemented by the periods Tb**1**, Tb**4**, Tc**1**, and Tc**4**, a monitoring period is implemented by the periods Tb**2**, Tb**5**, Tc**2**, and Tc**5**, and an AD conversion period is implemented by the periods Tb**3**, Tb**6**, Tc**3**, and Tc**6**.

[0208] During the detection preparation period Ta, the scanning line G**1**(*i*) is brought into an active state and the monitoring control line G**2**(*i*) is maintained in a non-active state. By this, the transistor T**1** goes into an on state and the transistor T**3** is maintained in an off state. In addition, during this period Ta, the control clock signals CLK**1**, CLK**2**, and CLK**2**B go to a high level, a high level, and an off level, respectively. Hence, the switches **333**, **334**, and **335** go into an on state, an on state, and an off state, respectively. In addition, during this period Ta, a potential Vmg is provided to the data signal line S(j) through the operational amplifier **331**. By performing writing based on the potential Vmg, the capacitor Cst is charged and the transistor T**2** goes into an on state. By the above, during the detection preparation period Ta, a drive current is supplied to the organic EL element OLED through the transistor T**2**, as indicated by an arrow denoted by reference character **72** in FIG. **13**. By this, the organic EL element OLED emits light at a luminance according to the drive current. Note, however, that the organic EL element OLED emits light for only a very short period of time.

[0209] When the period turns to the period Tb**1** (data signal line charging period), the scanning line G**1**(*i*) is brought into a non-active state and the monitoring control line G**2**(*i*) is brought into an active state. By this, the transistor T**1** goes into an off state and the transistor T**3** goes into an on state. Note that throughout the TFT characteristic detection period Tb, the transistor T**1** is maintained in the off state and the transistor T**3** is maintained in the on state. In addition, when the period turns to the period Tb**1**, a potential Vm_TFT is provided to the data signal line S(j) through the operational amplifier **331**. By the above, during the period Tb**1**, charging is performed such that the potential of the data signal line S(j) becomes Vm_TFT. Note that, as will be described later, during the period Tc**1** included in the OLED characteristic detection period Tc, charging is performed such that the potential of the data signal line S(j) becomes Vm_oled.

[0210] When the period turns to the period Tb**2** (monitoring period), the control clock signal CLK**1** changes from the high level to a low level. By this, the switch **333** goes into an off state. Here, when a threshold voltage of the transistor T**2** which is obtained based on an offset value stored in the TFT offset memory **51***a* is Vth(T**2**), the value of the potential Vmg, the value of the potential Vm_TFT, and the value of the potential Vm_oled are set such that the following expressions (1) and (2) hold true.

$$Vm\_TFT+Vth(T2)<Vmg \quad (1)$$

$$Vmg<Vm\_oled+Vth(T2) \quad (2)$$

In addition, when a light emission threshold voltage of the organic EL element OLED which is obtained based on an offset value stored in the OLED offset memory **51***b* is Vth(oled), the value of the potential Vm_TFT is set such that the following expression (3) holds true.

$$Vm\_TFT<ELVSS+Vth(oled) \quad (3)$$

Furthermore, when a breakdown voltage of the organic EL element OLED is Vbr(oled), the value of the potential Vm_TFT is set such that the following expression (4) holds true.

$$Vm\_TFT>ELVSS-Vbr(oled) \quad (4)$$

[0211] As described above, after performing writing based on the potential Vmg that satisfies the above expressions (1) and (2) during the detection preparation period Ta, the potential Vm_TFT that satisfies the above expressions (1), (3), and (4) is provided to the data signal line S(j) during the periods Tb**1** to Tb**2**. By the above expression (1), during the period Tb**2**, the transistor T**2** goes into an on state. In addition, by the above expressions (3) and (4), during the period Tb**2**, a current does not flow through the organic EL element OLED.

[0212] By the above, during the period Tb**2**, a current flowing through the transistor T**2** is outputted to the data signal line S(j) through the transistor T**3**, as indicated by an arrow denoted by reference character **73** in FIG. **14**. In addition, during the period Tb**2**, the switch **334** is in an on state. By this, charge is accumulated in the capacitor **332** according to the magnitude (time-integrated value) of the current (sink current) outputted to the data signal line S(j) during the period Tb**2**, and the potential of the output terminal of the operational amplifier **331** changes.

[0213] When the period turns to the period Tb**3** (AD conversion period), the control clock signal CLK**2** changes from the high level to the low level. By this, as shown in FIG. **15**, the switch **334** goes into an off state, and the data signal line S(j) and the internal data line Sin(j) go into an electrically disconnected state. As a result, analog data representing the magnitude of the current on the data signal line S(j) at an end time point of the period Tb**2** is held in the output and current-monitoring circuit **330**. In such a state, the selector **322** sequentially outputs analog data (monitored data MO) of a plurality of columns, by which each A/D converter **324** sequentially performs AD conversion on the analog data of a plurality of columns.

[0214] In addition, during the period Tb**3**, the control clock signal CLK**2**B changes from the low level to the high level. By this, as shown in FIG. **15**, the switch **335** goes into an on state and the data signal line S(j) and the control line CL go into an electrically connected state. As a result, during the period Tb**3**, charging is performed such that the potential

of the data signal line S(j) becomes Vm_TFT. In this manner, charging of the data signal line S(j) is performed through the control line CL during a period during which AD conversion is performed.

[0215] When the period turns to the period Tb**4** (data signal line charging period), the control clock signal CLK**1** changes from the low level to the high level, the control clock signal CLK**2** changes from the low level to the high level, and the control clock signal CLK**2**B changes from the high level to the low level. By this, the switches **333**, **334**, and **335** go into an on state, an on state, and an off state, respectively. In this manner, the switch **333** and the switch **334** go into an on state, and the potential Vm_TFT is provided to the data signal line S(j) through the operational amplifier **331**. By the above, during the period Tb**4**, recharging is performed such that the potential of the data signal line S(j) becomes Vm_TFT. Meanwhile, as described above, during the period Tb**3**, charging of the data signal line S(j) is performed through the control line CL. Hence, the period Tb**4** may be a period of very short length.

[0216] During the period Tb**5** (monitoring period), the same operation as that for the period Tb**2** is performed. During the period Tb**6** (AD conversion period), the same operation as that for the period Tb**3** is performed. In the above-described manner, with the voltage between the gate and source of the transistor T**2** set to a predetermined magnitude (Vmg−Vm_TFT), the magnitude of a current flowing between the drain and source of the transistor T**2** is repeatedly measured, by which a TFT characteristic is detected.

[0217] When the period turns to the period Tc**1** (data signal line charging period), the control clock signal CLK**1** changes from the low level to the high level, the control clock signal CLK**2** changes from the low level to the high level, and the control clock signal CLK**2**B changes from the high level to the low level. By this, the switches **333**, **334**, and **335** go into an on state, an on state, and an off state, respectively. In addition, in the present embodiment, as with the TFT characteristic detection period Tb, throughout the OLED characteristic detection period Tc, the transistor T**1** is maintained in the off state and the transistor T**3** is maintained in the on state. In addition, when the period turns to the period Tc**1**, a potential Vm_oled is provided to the data signal line S(j) through the operational amplifier **331**. By the above, during the period Tc**1**, charging is performed such that the potential of the data signal line S(j) becomes Vm_oled.

[0218] When the period turns to the period Tc**2** (monitoring period), the control clock signal CLK**1** changes from the high level to the low level. By this, the switch **333** goes into an off state. Here, the value of the potential Vm_oled is set such that the above expression (2) and the following expression (5) hold true.

$$ELVSS+Vth(oled)<Vm\_oled \tag{5}$$

In addition, when a breakdown voltage of the transistor T**2** is Vbr(T**2**), the value of the potential Vm_oled is set such that the following expression (6) holds true.

$$Vm\_oled<Vmg+Vbr(T2) \tag{6}$$

[0219] As described above, during the periods Tc**1** to Tc**2**, the potential Vm_oled that satisfies the above expressions (2), (5), and (6) is provided to the data signal line S(j). By the above expressions (2) and (6), during the period Tc**2**, the transistor T**2** goes into an off state. In addition, by the above expression (5), during the period Tc**2**, a current flows through the organic EL element OLED.

[0220] By the above, during the period Tc**2**, a current flows through the organic EL element OLED through the transistor T**3** from the data signal line S(j), as indicated by an arrow denoted by reference character **74** in FIG. **16**, and the organic EL element OLED emits light. Charge is accumulated in the capacitor **332** according to the magnitude (time-integrated value) of the current obtained at this time, and the potential of the output terminal of the operational amplifier **331** changes.

[0221] When the period turns to the period Tc**3**, the control clock signal CLK**2** changes from the high level to the low level. By this, as with the period Tb**3**, the switch **334** goes into an off state, and the data signal line S(j) and the internal data line Sin(j) go into an electrically disconnected state. As a result, analog data representing the magnitude of the current on the data signal line S(j) at an end time point of the period Tc**2** is held in the output and current-monitoring circuit **330**. In such a state, the selector **322** sequentially outputs analog data (monitored data MO) of a plurality of columns, by which each A/D converter **324** sequentially performs AD conversion on the analog data of a plurality of columns.

[0222] In addition, during the period Tc**3** (AD conversion period), the control clock signal CLK**2**B changes from the low level to the high level. By this, as with the period Tb**3**, the switch **335** goes into an on state and the data signal line S(j) and the control line CL go into an electrically connected state. As a result, during the period Tc**3**, charging is performed such that the potential of the data signal line S(j) becomes Vm_oled. In this manner, charging of the data signal line S(j) is performed through the control line CL during a period during which AD conversion is performed.

[0223] When the period turns to the period Tc**4** (data signal line charging period), the control clock signal CLK**1** changes from the low level to the high level, the control clock signal CLK**2** changes from the low level to the high level, and the control clock signal CLK**2**B changes from the high level to the low level. By this, the switches **333**, **334**, and **335** go into an on state, an on state, and an off state, respectively. In this manner, the switch **333** and the switch **334** go into an on state, and the potential Vm_oled is provided to the data signal line S(j) through the operational amplifier **331**. By the above, during the period Tc**4**, recharging is performed such that the potential of the data signal line S(j) becomes Vm_oled. Meanwhile, as described above, during the period Tc**3**, charging of the data signal line S(j) is performed through the control line CL. Hence, the period Tc**4** may be a period of very short length.

[0224] During the period Tc**5** (monitoring period), the same operation as that for the period Tc**2** is performed. During the period Tc**6** (AD conversion period), the same operation as that for the period Tc**3** is performed. In the above-described manner, the magnitude of a current flowing through the organic EL element OLED is repeatedly measured with the voltage between the anode and cathode of the organic EL element OLED set to a predetermined magnitude (Vm_oled−ELVSS), by which an OLED characteristic is detected.

[0225] Note that the value of the potential Vmg, the value of the potential Vm_TFT, and the value of the potential Vm_oled are determined taking also into account a current

measurable range of the adopted output and current-monitoring circuit **330**, etc., in addition to the above expressions (1) to (6).

[0226] When the period turns to the light emission preparation period Td, the scanning line G**1**(*i*) is brought into an active state and the monitoring control line G**2**(*i*) is brought into a non-active state. By this, the transistor T**1** goes into an on state and the transistor T**3** goes into an off state. In addition, during the light emission preparation period Td, the control clock signal CLK**1** changes from the low level to the high level, the control clock signal CLK**2** changes from the low level to the high level, and the control clock signal CLK**2**B changes from the high level to the low level. By this, the switches **333**, **334**, and **335** go into an on state, an on state, and an off state, respectively. In addition, during the light emission preparation period Td, a data potential D(i,j) according to a target luminance is provided to the data signal line S(j) through the operational amplifier **331**. By performing writing based on the data potential D(i,j), the capacitor Cst is charged and the transistor T**2** goes into an on state. By the above, during the light emission preparation period Td, a drive current is supplied to the organic EL element OLED through the transistor T**2**, as indicated by an arrow denoted by reference character **75** in FIG. **17**. By this, the organic EL element OLED emits light at a luminance according to the drive current.

[0227] During the light emission period TL (see FIG. **10**), the scanning line G**1**(*i*) is brought into a non-active state and the monitoring control line G**2**(*i*) is maintained in the non-active state. By this, the transistor T**1** goes into an off state and the transistor T**3** is maintained in the off state. Although the transistor T**1** goes into an off state, since the capacitor Cst is charged during the light emission preparation period Td by the writing based on the data potential D(i,j) according to the target luminance, the transistor T**2** is maintained in the on state. Therefore, during the light emission period TL, a drive current is supplied to the organic EL element OLED through the transistor T**2**, as indicated by an arrow denoted by reference character **76** in FIG. **18**. By this, the organic EL element OLED emits light at a luminance according to the drive current. That is, during the light emission period TL, the organic EL element OLED emits light according to the target luminance. Meanwhile, when the transistor T**1** goes into an off state, ideally, the gate potential of the transistor T**2** is held. However, in practice, due to second-order effects such as charge injection of the transistor T**1**, feedthrough of the scanning line G**1**(*i*), and charge distribution with a parasitic capacitance, the gate potential of the transistor T**2** changes from the written potential. On the other hand, immediately before the TFT characteristic detection period Tb which precedes the light emission period TL, too, the transistor T**1** goes into an off state and the gate of the transistor T**2** goes into a hold state, and thus, the influences of the second-order effects during the TFT characteristic detection period Tb and during the light emission period TL become substantially equal to each other. Accordingly, even when the magnitude of the influence of the second-order effects varies between pixels (due to variations in parasitic capacitance value, etc.), detection of a TFT characteristic is performed taking into account the second-order effects and correction is performed. Thus, variations in second-order effects between pixels can be canceled out each other.

[0228] As described above, in a non-monitored row, a process of allowing an organic EL element OLED to emit light is performed as with a common organic EL display device. On the other hand, in a monitored row, a process for detecting a TFT characteristic and an OLED characteristic is performed and then a process of allowing an organic EL element OLED to emit light is performed. Therefore, as can be grasped from FIG. **19**, the length of a light emission period for the monitored row is shorter than that of a light emission period for the non-monitored row. Hence, the magnitude of the data potential D(i, j) to be applied to the data signal line S(j) during the light emission preparation period Td is adjusted such that an integrated luminance during a frame period is equal to a luminance appearing in the non-monitored row. Specifically, a data potential corresponding to a grayscale voltage slightly larger than a grayscale voltage for the non-monitored row is provided to the data signal line S(j) during the light emission preparation period Td. In other words, with any organic EL element OLED defined as a focused organic EL element, when the focused organic EL element is included in the monitored row, during the light emission preparation period Td, a data potential corresponding to a larger grayscale voltage than a grayscale voltage provided when the focused organic EL element is included in the non-monitored row is provided by the source driver **30** to the data signal line S(j). By this, a degradation in display quality is suppressed.

[0229] Note that although in the present embodiment, current measurement for detecting a TFT characteristic is performed twice during a TFT characteristic detection period Tb, and current measurement for detecting an OLED characteristic is performed twice during an OLED characteristic detection period Tc, the present invention is not limited thereto. Each of current measurement for detecting a TFT characteristic and current measurement for detecting an OLED characteristic may be performed once or may be performed three times or more during a TFT characteristic detection period Tb and an OLED characteristic detection period Tc. In addition, the number of times current measurement for detecting a TFT characteristic is performed may be different from the number of times current measurement for detecting an OLED characteristic is performed. In addition, there may be a frame having only a TFT characteristic detection period Tb or there may be a frame having only an OLED characteristic detection period Tc. That is, only either one of detection of a TFT characteristic and detection of an OLED characteristic may be performed per frame period. In this case, during a frame period during which detection of a TFT characteristic is performed, a potential Vm_TFT is provided to the data signal line S(j) throughout periods represented by Tb to Tc in FIG. **10**, and during a frame period during which detection of an OLED characteristic is performed, a potential Vm_oled is provided to the data signal line S(j) throughout the periods represented by Tb to Tc in FIG. **10**. By doing so, sufficient time for transferring monitored data MO obtained by AD conversion to the control circuit **20** is ensured after the AD conversion.

[0230] In addition, although in the present embodiment, as shown in FIG. **9**, every time a frame is changed, a monitored row is also changed, the present invention is not limited thereto. The same row may be set as a monitored row over a plurality of frames. For example, it is also possible to set the same row as a monitored row over a total of four frames

including two frames where characteristic detection of the transistor T2 (drive transistor) is performed using two types of Vm_TFT, and two frames where characteristic detection of an organic EL element OLED (electrooptical element) is performed using two types of Vm_oled. Furthermore, the same row may be set as a monitored row over a plurality of frames using the same monitoring voltages (Vm_TFT and Vm_oled). By thus repeatedly performing a characteristic detection process on one row, an effect of an improvement in S/N ratio can be obtained. Furthermore, although in the present embodiment only one row is set as a monitored row in each frame, the present invention is not limited thereto. Within a range where display quality is not degraded, a plurality of rows may be set as monitored rows in each frame, or characteristic detection for all rows may be continuously performed immediately after the power to a panel is turned on or during a power-off period or at any timing during a non-display period.

[0231] <3.3 Update to Correction Data in the Correction Data Storage Unit>

[0232] Next, a description will be made of how correction data (offset values stored in the TFT offset memory **51***a*, offset values stored in the OLED offset memory **51***b*, gain values stored in the TFT gain memory **52***a*, and degradation correction factors stored in the OLED gain memory **52***b*) stored in the correction data storage unit **50** is updated. FIG. **20** is a flowchart for describing a procedure for updating correction data in the correction data storage unit **50**. Note that here correction data corresponding to one pixel is focused.

[0233] First, detection of a TFT characteristic is performed during a TFT characteristic detection period Tb (step S**110**). By this step S**110**, an offset value and a gain value for correcting a video signal are obtained. Then, the offset value obtained at step S**110** is stored in the TFT offset memory **51***a*, as a new offset value (step S**120**). In addition, the gain value obtained at step S**110** is stored in the TFT gain memory **52***a*, as a new gain value (step S**130**). Thereafter, detection of an OLED characteristic is performed during an OLED characteristic detection period Tc (step S**140**). By this step S**140**, an offset value and a degradation correction factor for correcting the video signal are obtained. Then, the offset value obtained at step S**140** is stored in the OLED offset memory **51***b*, as a new offset value (step S**150**). In addition, the degradation correction factor obtained at step S**140** is stored in the OLED gain memory **52***b*, as a new degradation correction factor (step S**160**). In the above-described manner, an update to correction data corresponding to one pixel is performed. In the present embodiment, detection of a TFT characteristic and an OLED characteristic for one row is performed in each frame, and thus, m offset values in the TFT offset memory **51***a*, m gain values in the TFT gain memory **52***a*, m offset values in the OLED offset memory **51***b*, and m degradation correction factors in the OLED gain memory **52***b* are updated per frame period.

[0234] Note that, in the present embodiment, characteristic data is implemented by data (offset values, a gain value, and a degradation correction factor) which is obtained based on results of detection at step S**110** and step S**140**.

[0235] Meanwhile, as described above, during the OLED characteristic detection period Tc, measurement of the magnitude of a current flowing through the organic EL element OLED is performed based on a certain voltage (Vm_oled−ELVSS). The smaller the detected current which is a result of the measurement, the larger the degree of degradation of the organic EL element OLED. Therefore, an update to data in the OLED offset memory **51***b* and the OLED gain memory **52***b* is performed such that the smaller the detected current, the larger the offset value and the larger the degradation correction factor.

[0236] <3.4 Correction of a Video Signal>

[0237] In the present embodiment, in order to compensate for degradation of a drive transistor and degradation of an organic EL element OLED, correction of a video signal transmitted from an external source is performed using correction data stored in the correction data storage unit **50**. The correction of the video signal will be described below with reference to FIG. **21**.

[0238] As shown in FIG. **21**, the control circuit **20** is provided with a LUT **211**, a multiplying unit **212**, a multiplying unit **213**, an adding unit **214**, an adding unit **215**, and a multiplying unit **216**, as components for correcting the video signal. In addition, the control circuit **20** is provided with a multiplying unit **221** and an adding unit **222**, as components for correcting a potential Vm_oled which is provided to the data signal line S during the OLED characteristic detection period Tc. A CPU **230** in the control circuit **20** performs, for example, control of the operation of the above-described components, update and reading of data in each memory (the TFT offset memory **51***a*, the TFT gain memory **52***a*, the OLED offset memory **51***b*, and the OLED gain memory **52***b*) in the correction data storage unit **50**, update and reading of data in a nonvolatile memory **70**, and giving and receiving of data to/from the source driver **30**.

[0239] In a configuration such as that described above, a video signal transmitted from an external source is corrected as follows. First, gamma correction is performed on the video signal transmitted from an external source, using the LUT **211**. Specifically, a grayscale P represented by the video signal is converted into a control voltage Vc by gamma correction. The multiplying unit **212** receives the control voltage Vc and a gain value B**1** read from the TFT gain memory **52***a*, and outputs the value "Vc·B**1**" which is obtained by multiplying the control voltage Vc and the gain value B**1** together. The multiplying unit **213** receives the value "Vc·B**1**" outputted from the multiplying unit **212** and a degradation correction factor B**2** read from the OLED gain memory **52***b*, and outputs the value "Vc·B**1**·B**2**" which is obtained by multiplying the value "Vc·B**1**" and the degradation correction factor B**2** together. The adding unit **214** receives the value "Vc·B**1**·B**2**" outputted from the multiplying unit **213** and an offset value Vt**1** read from the TFT offset memory **51***a*, and outputs the value "Vc·B**1**·B**2**+Vt**1**" which is obtained by adding the value "Vc·B**1**·B**2**" and the offset value Vt**1** together. The adding unit **215** receives the value "Vc·B**1**·B**2**+Vt**1**" outputted from the adding unit **214** and an offset value Vt**2** read from the OLED offset memory **51***b*, and outputs the value "Vc·B**1**·B**2**+Vt**1**+Vt**2**" which is obtained by adding the value "Vc·B**1**·B**2**+Vt**1**" and the offset value Vt**2** together. The multiplying unit **216** receives the value "Vc·B**1**·B**2**+Vt**1**+Vt**2**" outputted from the adding unit **215** and a coefficient Z for compensating for attenuation of a data potential caused by a parasitic capacitance in the pixel circuit **11**, and outputs the value "Z (Vc·B**1**·B**2**+Vt**1**+Vt**2**)" which is obtained by multiplying the value "Vc·B**1**·B**2**+Vt**1**+Vt**2**" and the coefficient Z together. The value "Z (Vc·B**1**·B**2**+Vt**1**+Vt**2**)" obtained in the above-described manner is transmitted as a data signal DA to the source

driver **30** from the control circuit **20**. A potential Vmg which is provided to the data signal line S during the detection preparation period Ta is also corrected by the same process as that for the video signal. Note that the multiplying unit **216** that performs a process of multiplying a value outputted from the adding unit **215** by the coefficient Z for compensating for attenuation of a data potential does not necessarily need to be provided.

[0240] In addition, a potential Vm_oled which is provided to the data signal line S during the OLED characteristic detection period Tc is corrected as follows. The multiplying unit **221** receives pre_Vm_oled (Vm_oled before correction) and a degradation correction factor B**2** read from the OLED gain memory **52***b*, and outputs the value "pre_Vm_oled·B**2**" which is obtained by multiplying pre_Vm_oled and the degradation correction factor B**2** together. The adding unit **222** receives the value "pre_Vm_oled·B**2**" outputted from the multiplying unit **221** and an offset value Vt**2** read from the OLED offset memory **51***b*, and outputs the value "pre_Vm_oled·B**2**+Vt**2**" which is obtained by adding the value "pre_Vm_oled·B**2**" and the offset value Vt**2** together. The value "pre_Vm_oled·B**2**+Vt**2**" obtained in the above-described manner is transmitted to the source driver **30** from the control circuit **20**, as data indicating the potential Vm_oled of the data signal line S provided during the OLED characteristic detection period Tc.

[0241] <3.5 Summary of the Drive Method>

[0242] FIG. **22** is a flowchart for describing an outline of operation related to detection of a TFT characteristic and an OLED characteristic. First, detection of a TFT characteristic is performed during the TFT characteristic detection period Tb (step S**210**). Then, using a result of the detection at step S**210**, an update to the TFT offset memory **51***a* and the TFT gain memory **52***a* is performed (step S**220**). Subsequently, detection of an OLED characteristic is performed during the OLED characteristic detection period Tc (step S**230**). Then, using a result of the detection at step S**230**, an update to the OLED offset memory **51***b* and the OLED gain memory **52***b* is performed (step S**240**). Thereafter, correction of a video signal transmitted from an external sources is performed using the correction data stored in the TFT offset memory **51***a*, the TFT gain memory **52***a*, the OLED offset memory **51***b*, and the OLED gain memory **52***b* (step S**250**).

[0243] Note that in the present embodiment a characteristic detecting step is implemented by step S**210** and step S**230**, a correction data storing step is implemented by step S**220** and step S**240**, and a video signal correcting step is implemented by step S**250**.

[0244] <4. Effects>

[0245] According to the present embodiment, detection of a TFT characteristic and an OLED characteristic for one row is performed in each frame. One horizontal scanning period THm for a monitored row is longer than one horizontal scanning period THn for a non-monitored row, and in the monitored row, detection of a TFT characteristic and detection of an OLED characteristic are performed during the one horizontal scanning period THm. Then, a video signal transmitted from an external source is corrected using correction data which is obtained by taking into account both of a result of the detection of a TFT characteristic and a result of the detection of an OLED characteristic. Since a data potential based on the thus corrected video signal is applied to a data signal line S, when an organic EL element OLED in each pixel circuit **11** is allowed to emit light, a drive current of a magnitude that compensates for degradation of the drive transistor (transistor T**2**) and degradation of the organic EL element OLED is supplied to the organic EL element OLED (see FIG. **23**). In addition, by increasing a current in accordance with a degradation level of a pixel with the lowest degradation as shown in FIG. **24**, it becomes possible to compensate for burn-in. Here, the data signal line S in the present embodiment is not only used as a signal line that transfers a luminance signal for allowing an organic EL element OLED in each pixel circuit **11** to emit light at a desired luminance, but also used as a signal line for characteristic detection (a signal line that provides control potentials (Vmg, Vm_TFT, and Vm_oled) for characteristic detection to the pixel circuit **11**, and a signal line serving as a path for currents that represent characteristics and that are measurable by the output and current-monitoring circuit **330**). That is, new signal lines do not need to be provided in the display unit **10** to detect a TFT characteristic and an OLED characteristic. Accordingly, it becomes possible to simultaneously compensate for both of degradation of the drive transistors (transistors T**2**) and degradation of the organic EL elements OLED while an increase in circuit size is suppressed.

[0246] In addition, in the present embodiment, the output and current-monitoring circuits **330** provided for the respective columns have the function of holding analog data representing a TFT characteristic and an OLED characteristic (sample and hold function). Using the sample and hold function, an A/D converter **324** for converting the above-described analog data into digital data is shared between a plurality of columns. This effectively suppresses an increase in circuit size associated with implementation of a configuration capable of detecting characteristics of the circuit elements. In addition, each output and current-monitoring circuit **330** is provided with a switch **334** for controlling a connection state between a data signal line S and an internal data line Sin, and a switch **335** for controlling a connection state between the data signal line S and a predetermined control line CL. Then, during a period during which AD conversion by the A/D converter **324** is performed, the data signal line S and the internal data line Sin are electrically disconnected from each other, and a predetermined potential (Vm_TFT or Vm_oled) is provided to the data signal line S from the control line CL. By this, the potential of the data signal line S is prevented from being changed during AD conversion due to sharing of the A/D converter **324**. Due to this fact, since recharging of the data signal line S is performed in a very short period of time, it becomes possible to repeatedly perform current measurement for characteristic detection. By this, an effect that a sufficient S/N ratio can be ensured is obtained.

[0247] Furthermore, in the present embodiment, oxide TFTs (specifically, TFTs having an In—Ga—Zn—O-based semiconductor layer) are adopted as the transistors T**1** to T**3** in the pixel circuit **11**. In terms of this, too, an effect that a sufficient S/N ratio can be ensured is obtained. This will be described below. Note that here a TFT having an In—Ga—Zn—O-based semiconductor layer is referred to as "In—Ga—Zn—O-TFT". Comparing the In—Ga—Zn—O-TFT with an LTPS (Low Temperature Poly silicon)-TFT, the off-current is extremely smaller in the In—Ga—Zn—O-TFT than in the LTPS-TFT. For example, when the LTPS-TFT is adopted as the transistor T**3** in the pixel circuit **11**, the off-current is about 1 pA at the maximum. On the other hand,

when the In—Ga—Zn—O-TFT is adopted as the transistor T**3** in the pixel circuit **11**, the off-current is about 10 fA at the maximum. Therefore, for example, the off-current for 1000 rows is about 1 nA at the maximum for a case of adopting the LTPS-TFTs, and is about 10 pA at the maximum for a case of adopting the In—Ga—Zn—O-TFTs. A detected current is about 10 to 100 nA for both cases. Meanwhile, each data signal line S is connected to transistors T**3** in pixel circuits **11** of all rows of a corresponding column. Therefore, the S/N ratio of the data signal line S for when characteristic detection is performed depends on a total of leakage currents of transistors T**3** in non-monitored rows. Specifically, the S/N ratio of the data signal line S for when characteristic detection is performed is expressed by "detected current/(leakage current×the number of non-monitored rows)". From the above fact, for example, in an organic EL display device having a display unit **10** with "Landscape FHD", the S/N ratio is about 10 for a case of adopting the LTPS-TFTs, and is about 1000 for a case of adopting the In—Ga—Zn—O-TFTs. As such, in the present embodiment, a sufficient S/N ratio can be ensured when current detection is performed.

[0248] <5. Variants>

[0249] Variants of the above-described embodiment will be described below. Note that in the following only different points from the above-described embodiment will be described in detail, and a description of the same points as in the above-described embodiment is omitted.

[0250] <5.1 First Variant>

[0251] In the above-described embodiment, a potential that is provided to the data signal line S during the OLED characteristic detection period Tc is corrected based on an offset value Vt**2** stored in the OLED offset memory **51***b* and a degradation correction factor B**2** stored in the OLED gain memory **52***b* (see FIG. **21**). That is, the magnitude of a potential Vm_oled can vary between pixels. In this regard, since the switch **334** goes into an off state during AD conversion as described above, there is a need to provide a different D/A converter than the D/A converter **321** shown in FIG. **1** in order to supposedly supply a potential Vm_oled whose magnitude varies between pixels to the data signal line S from the control line CL.

[0252] However, if recharging of the data signal line S after AD conversion is performed in a short period of time, then the potential Vm_oled which is set for each pixel does not necessarily need to be supplied to the data signal line S from the control line CL. Hence, in the present variant, during the OLED characteristic detection period Tc, a certain potential close to the potential Vm_oled is provided to the control line CL from the power supply circuit. By this, during the OLED characteristic detection period Tc, the certain potential is provided to the data signal line S from the control line CL.

[0253] As described above, as long as the magnitude of a potential provided to the control line CL during the OLED characteristic detection period Tc is substantially equal to that of a potential Vm_oled which is set for each pixel, the magnitude may be exactly the same as the potential Vm_oled or may be a potential close to the potential Vm_oled.

[0254] <5.2 Second Variant>

[0255] In the above-described embodiment, the configuration is such that during periods (a period Tc**3** and a period Tc**6**) during which AD conversion is performed within the OLED characteristic detection period Tc, a potential Vm_oled is provided to the data signal line S from a control line CL. However, the present invention is not limited thereto. A configuration (a configuration of the present variant) can also be adopted in which during the periods during which AD conversion is performed within the OLED characteristic detection period Tc, the data signal line S is brought into a high-impedance state. A drive method in the present variant will be described below, mainly for different points from the above-described embodiment.

[0256] FIG. **25** is a timing chart for describing the operation of a pixel circuit **11** (assumed to be a pixel circuit **11** at an ith row and a jth column) included in a monitored row in the present variant. As can be grasped from FIGS. **10** and **25**, the waveform of the monitoring control line G**2**(*i*) during the OLED characteristic detection period Tc is different between the above-described embodiment and the present variant.

[0257] FIG. **26** is a timing chart for describing details of one horizontal scanning period THm for a monitored row. With reference to this FIG. **26**, characteristic detection operation in the present variant will be described. During the detection preparation period Ta, the TFT characteristic detection period Tb, and the light emission preparation period Td, the same operation as that in the above-described embodiment is performed, and thus, a description thereof is omitted.

[0258] As with the above-described embodiment, the OLED characteristic detection period Tc is composed of periods Tc**1** to Tc**6**. During the period Tc**1** (data signal line charging period) and the period Tc**2** (monitoring period), the same operation as that in the above-described embodiment is performed. When the period turns to the period Tc**3** (AD conversion period), the control clock signal CLK**2** changes from the high level to the low level. By this, the switch **334** goes into an off state, and the data signal line S(j) and the internal data line Sin(j) go into an electrically disconnected state. Then, in the same manner as in the above-described embodiment, each A/D converter **324** sequentially performs AD conversion on analog data of a plurality of columns. In addition, during the period Tc**3**, unlike the above-described embodiment, the control clock signal CLK**2**B is maintained at a low level and the monitoring control line G**2**(*i*) is brought into a non-active state. By this, the switch **335** is maintained in an off state and the transistor T**3** also goes into an off state. By the above, during the period Tc**3**, the data signal line S(j) goes into a high-impedance state. In this manner, during the period Tc**3**, a leak of charge from the data signal line S(j) is prevented and the potential of the data signal line S(j) is maintained at a potential close to Vm_oled.

[0259] During the period Tc**4** (data signal line charging period), in the same manner as in the above-described embodiment, recharging of the data signal line S(j) is performed. As described above, during the period Tc**3**, the data signal line S(j) goes into a high-impedance state and the potential of the data signal line S(j) is maintained at a potential close to Vm_oled. Thus, during the period Tc**4**, recharging is performed in a very short period of time such that the potential of the data signal line S(j) becomes Vm_oled. During the period Tc**5** (monitoring period), the same operation as that for the period Tc**2** is performed. During the period Tc**6** (AD conversion period), the same operation as that for the period Tc**3** is performed.

[0260] As described above, according to the present variant, during periods during which AD conversion by the A/D

converter **324** is performed in the OLED characteristic detection period Tc, the data signal line S is brought into a high-impedance state. In addition, during periods during which AD conversion by the A/D converter **324** is performed in the TFT characteristic detection period Tb, as with the above-described embodiment, a predetermined potential (Vm_TFT) is provided to the data signal line S from the control line CL. By this, in the present variant, too, recharging of the data signal line S is performed in a very short period of time. Accordingly, it becomes possible to repeatedly perform current measurement for characteristic detection, enabling to ensure a sufficient S/N ratio.

[0261] Note that the data signal line S(j) can be brought into a high-impedance state by bringing the transistor T**3** into an off state also during periods (the period Tb**3** and the period Tb**6**) during which AD conversion is performed within the TFT characteristic detection period Tb. A circuit configuration for this case is one in which the control line CL and the switch **335** are removed from the configuration shown in FIG. **1** (see FIG. **27**). Note, however, that in this case since the transistor T**2** is in an on state, a current is supplied to the organic EL element OLED and thus the organic EL element OLED emits light. In addition, since the source potential of the transistor T**2** significantly changes, a recharging period after AD conversion needs to be increased. Therefore, it is preferred that during the periods during which AD conversion is performed within the TFT characteristic detection period Tb, as with the above-described embodiment, a potential Vm_TFT be provided to the data signal line S(j) from the control line CL while the transistor T**3** is maintained in an on state. However, also in the case of adopting the configuration shown in FIG. **27**, there are obtained an effect that an A/D converter **324** can be shared between a plurality of columns, an effect that a recharging period for when an OLED characteristic is detected can be reduced, and an effect that the circuit size can be reduced compared to the case of adopting the configuration shown in FIG. **1**.

[0262] <5.3 Third Variant>

[0263] In general, in an organic EL display device, one frame period includes a vertical scanning period which is a period during which writing of video signals to pixels is sequentially performed in order from the first row to the last row; and a vertical retrace period (vertical synchronization period) which is a period provided to bring writing of video signals back to the first row from the last row. Then, during the operation of the organic EL display device, a vertical scanning period Tv and a vertical retrace period Tf are repeated alternately as shown in FIG. **28**. Meanwhile, in the above-described embodiment, detection of a TFT characteristic and detection of an OLED characteristic are performed during the vertical scanning period Tv. However, the present invention is not limited thereto. A configuration (a configuration of the present variant) can also be adopted in which detection of a TFT characteristic and detection of an OLED characteristic are performed during the vertical retrace period Tf.

[0264] In the present variant, for example, assuming that detection of a TFT characteristic and an OLED characteristic for the first row is performed during a vertical retrace period Tf in a (k+1)th frame, detection of a TFT characteristic and an OLED characteristic for the second row is performed during a vertical retrace period Tf in a (k+2)th frame, detection of a TFT characteristic and an OLED characteristic for the third row is performed during a vertical retrace period Tf in a (k+3)th frame, and detection of a TFT characteristic and an OLED characteristic for an nth row is performed during a vertical retrace period Tf in a (k+n)th frame. That is, every time a frame is changed, a monitored row is also changed. Note that during the vertical scanning period Tv, the same operation as that of a common organic EL display device is performed.

[0265] FIG. **29** is a timing chart for describing the operation, during a vertical retrace period Tf, of a pixel circuit **11** (assumed to be a pixel circuit **11** at an ith row and a jth column) included in a monitored row in the present variant. As shown in FIG. **29**, in the present variant, apart of the vertical retrace period Tf serves as a characteristic detection processing period including a detection preparation period Ta, a TFT characteristic detection period Tb, an OLED characteristic detection period Tc, and a light emission preparation period Td.

[0266] FIG. **30** is a timing chart for describing details of a vertical retrace period Tf in the present variant. As can be grasped from FIG. **30**, during a detection preparation period Ta, a TFT characteristic detection period Tb (Tb**1** to Tb**6**), and a light emission preparation period Td included in the vertical retrace period Tf in the present variant, the same operation as that for the detection preparation period Ta, the TFT characteristic detection period Tb (Tb**1** to Tb**6**), and the light emission preparation period Td in the above-described embodiment is performed (the above-described second variant is also the same). During an OLED characteristic detection period Tc (Tc**1** to Tc**6**) included in the vertical retrace period Tf in the present variant, the same operation as that for the OLED characteristic detection period Tc (Tc**1** to Tc**6**) in the above-described second variant is performed. In this manner, it is also possible to perform detection of a TFT characteristic and an OLED characteristic during the vertical retrace period Tf instead of the vertical scanning period Tv. Note that the configuration may be such that the same operation as that for the OLED characteristic detection period Tc in the above-described embodiment is performed during the OLED characteristic detection period Tc in the present variant.

[0267] Meanwhile, in the non-monitored row, writing according to a target luminance is performed during a selection period included in the vertical scanning period Tv, and light emission of the organic EL element OLED based on the writing continues for substantially one frame period. On the other hand, in the monitored row, writing is performed during a selection period included in the vertical scanning period Tv, but when the period turns to the vertical retrace period Tf, light emission of the organic EL element OLED is temporarily suspended. Hence, in order for the organic EL element OLED to emit light in the monitored row after the vertical retrace period Tf ends, writing based on a data potential D (i, j) is performed during a light emission preparation period Td included in the vertical retrace period Tf.

[0268] Specifically, in the monitored row, as shown in FIG. **31**, first, the organic EL element OLED emits light based on writing performed during the selection period included in the vertical scanning period Tv in a preceding frame. Thereafter, the organic EL element OLED is temporarily turned off during the vertical retrace period Tf. Thereafter, the organic EL element OLED emits light based on writing performed during the light emission preparation

period Td included in the vertical retrace period Tf. In this regard, in order to enable writing based on a data potential D(i, j) during the light emission preparation period Td, corresponding data needs to be held after the writing performed during the selection period included in the vertical scanning period Tv. Regarding this point, since the data to be held is merely data for one line, an increase in memory capacity is a little. On the other hand, in the above-described embodiment, since the length of one horizontal scanning period is different between a monitored row and a non-monitored row, a line memory for several tens of lines may be required depending on the timing of data transfer from the control circuit **20**. By the above, according to the present variant, required memory capacity is reduced compared to the above-described embodiment.

[0269] Note that taking into account the fact that light emission of the organic EL element OLED in the monitored row is temporarily suspended during the vertical retrace period Tf, a data potential corresponding to a larger grayscale voltage than an original grayscale voltage may be provided in advance to the data signal line S during a selection period (a period denoted by reference character Tz in FIG. **31**) included in the vertical scanning period Tv. In other words, with any organic EL element OLED defined as a focused organic EL element, when the focused organic EL element is included in the monitored row, during the selection period included in the vertical scanning period Tv, a data potential corresponding to a larger grayscale voltage than a grayscale voltage provided when the focused organic EL element is included in the non-monitored row may be provided by the source driver **30** to the data signal line S(j). By this, a degradation in display quality is suppressed.

[0270] <6. Others>

[0271] The present invention is not limited to the above-described embodiment and variants and may be implemented by making various modifications thereto without departing from the true scope and spirit of the present invention. For example, an organic EL display device to which the present invention can be applied is not limited to one including the pixel circuits **11** which are exemplified in the above-described embodiment. A pixel circuit may have other configurations than that exemplified in the above-described embodiment, as long as the pixel circuit includes at least an electrooptical element (organic EL element OLED) that is controlled by a current, transistors T**1** to T**3**, and a capacitor Cst.

DESCRIPTION OF REFERENCE CHARACTERS

[0272] **1**: ORGANIC EL DISPLAY DEVICE
[0273] **10**: DISPLAY UNIT
[0274] **11**: PIXEL CIRCUIT
[0275] **20**: CONTROL CIRCUIT
[0276] **30**: SOURCE DRIVER
[0277] **31**: DRIVE SIGNAL GENERATING CIRCUIT
[0278] **32**: SIGNAL CONVERSION CIRCUIT
[0279] **33**: OUTPUT UNIT
[0280] **40**: GATE DRIVER
[0281] **50**: CORRECTION DATA STORAGE UNIT
[0282] **51***a*: TFT OFFSET MEMORY
[0283] **51***b*: OLED OFFSET MEMORY
[0284] **52***a*: TFT GAIN MEMORY
[0285] **52***b*: OLED GAIN MEMORY
[0286] **321**: D/A CONVERTER
[0287] **322**: SELECTOR
[0288] **323**: OFFSET CIRCUIT
[0289] **324**: A/D CONVERTER
[0290] **330**: OUTPUT AND CURRENT-MONITORING CIRCUIT
[0291] **333** to **335**: SWITCH
[0292] T**1** to T**3**: TRANSISTOR
[0293] Cst: CAPACITOR
[0294] G**1** and G**1**(**1**) to G**1**(*n*): SCANNING LINE
[0295] G**2** and G**2**(**1**) to G**2**(*n*): MONITORING CONTROL LINE
[0296] S, S(j), and S(**1**) to S(m): DATA SIGNAL LINE
[0297] Sin, Sin(j), and Sin(**1**) to Sin(m): INTERNAL DATA LINE
[0298] ELVDD: HIGH-LEVEL POWER SUPPLY VOLTAGE, HIGH-LEVEL POWER SUPPLY LINE
[0299] ELVSS: LOW-LEVEL POWER SUPPLY VOLTAGE, LOW-LEVEL POWER SUPPLY LINE
[0300] Ta: DETECTION PREPARATION PERIOD
[0301] Tb: TFT CHARACTERISTIC DETECTION PERIOD
[0302] Tc: OLED CHARACTERISTIC DETECTION PERIOD
[0303] Tb**1**, Tb**4**, Tc**1**, and Tc**4**: DATA SIGNAL LINE CHARGING PERIOD
[0304] Tb**2**, Tb**5**, Tc**2**, and Tc**5**: MONITORING PERIOD
[0305] Tb**3**, Tb**6**, Tc**3**, and Tc**6**: AD CONVERSION PERIOD
[0306] Td: LIGHT EMISSION PREPARATION PERIOD
[0307] TL: LIGHT EMISSION PERIOD

1-13. (canceled).

14. An active matrix-type display device comprising:

a display unit having: a pixel matrix of n rows×m columns including n×m pixel circuits (n and m are integers greater than or equal to 2), each pixel circuit including an electrooptical element whose luminance is controlled by a current and a drive transistor for controlling a current to be supplied to the electrooptical element; scanning lines provided for the respective rows of the pixel matrix; monitoring control lines provided for the respective rows of the pixel matrix; and data signal lines provided for the respective columns of the pixel matrix;

a pixel circuit driving unit configured to drive the scanning lines, the monitoring control lines, and the data signal lines such that a characteristic detection process is performed during a frame period and that each electrooptical element emits light according to a target luminance, the characteristic detection process detecting a characteristic of a characteristic detection target circuit element including at least one of the electrooptical element and the drive transistor;

a correction data storage unit configured to store characteristic data obtained based on results of the characteristic detection process, as correction data for correcting video signals; and

a video signal correcting unit configured to generate data signals to be supplied to the n×m pixel circuits by correcting the video signals based on the correction data stored in the correction data storage unit, wherein

each of the pixel circuits includes:

the electrooptical element;

an input transistor having a control terminal connected to the scanning line, a first conduction terminal

connected to a control terminal of the drive transistor, and a second conduction terminal connected to the data signal line;

the drive transistor having a first conduction terminal to which a drive power supply potential is provided;

a monitoring control transistor having a control terminal connected to the monitoring control line, a first conduction terminal connected to a second conduction terminal of the drive transistor and an anode of the electrooptical element, and a second conduction terminal connected to the data signal line; and

a first capacitor having one end connected to the control terminal of the drive transistor to hold a potential of the control terminal of the drive transistor,

the pixel circuit driving unit includes:

an output and current-monitoring circuit having a function of applying the data signal to the data signal line and a function of obtaining, as monitored data, data according to a magnitude of a current flowing through the data signal line, the monitored data being base data for the characteristic data; and

an AD conversion circuit configured to convert the monitored data from an analog value to a digital value,

the output and current-monitoring circuit includes:

an internal data line connected to the data signal line;

an operational amplifier having a non-inverting input terminal to which the data signal is provided, and an inverting input terminal connected to the internal data line;

a second capacitor having one end connected to the internal data line, and an other end connected to an output terminal of the operational amplifier;

a first control switch having one end connected to the internal data line, and an other end connected to the output terminal of the operational amplifier; and

a second control switch having one end connected to the data signal line, and an other end connected to the internal data line,

the AD conversion circuit is provided per plurality of the output and current-monitoring circuits,

when a row for which the characteristic detection process is performed during a frame period is defined as a monitored row, and a row other than the monitored row is defined as a non-monitored row, the frame period includes a characteristic detection processing period including: a detection preparation period during which preparation for detecting a characteristic of the characteristic detection target circuit element is performed in the monitored row; a current measurement period during which a characteristic of the characteristic detection target circuit element is detected by measuring a current flowing through the data signal line; and a light emission preparation period during which preparation for allowing the electrooptical element to emit light is performed in the monitored row,

the current measurement period includes: a data signal line charging period during which the data signal line is charged such that a current of a magnitude according to the characteristic of the characteristic detection target circuit element flows through the data signal line; a monitoring period during which the monitored data is obtained by accumulating a time-integrated value of the current flowing through the data signal line in the second capacitor; and an AD conversion period during which the AD conversion circuit converts the monitored data from the analog value to the digital value, and

during the AD conversion period,

the data signal line and the internal data line are electrically disconnected from each other by bringing the second control switch into an off state, and

the AD conversion circuit sequentially converts the plurality of pieces of monitored data from analog values to digital values, the plurality of pieces of monitored data being obtained by a plurality of corresponding output and current-monitoring circuits.

15. An active matrix-type display device comprising:

a display unit having: a pixel matrix of n rows×m columns including n×m pixel circuits (n and m are integers greater than or equal to 2), each pixel circuit including an electrooptical element whose luminance is controlled by a current and a drive transistor for controlling a current to be supplied to the electrooptical element; scanning lines provided for the respective rows of the pixel matrix; monitoring control lines provided for the respective rows of the pixel matrix; and data signal lines provided for the respective columns of the pixel matrix;

a pixel circuit driving unit configured to drive the scanning lines, the monitoring control lines, and the data signal lines such that a characteristic detection process is performed during a frame period and that each electrooptical element emits light according to a target luminance, the characteristic detection process detecting a characteristic of a characteristic detection target circuit element including at least one of the electrooptical element and the drive transistor;

a correction data storage unit configured to store characteristic data obtained based on results of the characteristic detection process, as correction data for correcting video signals; and

a video signal correcting unit configured to generate data signals to be supplied to the n×m pixel circuits by correcting the video signals based on the correction data stored in the correction data storage unit, wherein

each of the pixel circuits includes:

the electrooptical element;

an input transistor having a control terminal connected to the scanning line, a first conduction terminal connected to a control terminal of the drive transistor, and a second conduction terminal connected to the data signal line;

the drive transistor having a first conduction terminal to which a drive power supply potential is provided;

a monitoring control transistor having a control terminal connected to the monitoring control line, a first conduction terminal connected to a second conduction terminal of the drive transistor and an anode of the electrooptical element, and a second conduction terminal connected to the data signal line; and

a first capacitor having one end connected to the control terminal of the drive transistor to hold a potential of the control terminal of the drive transistor,

the pixel circuit driving unit includes:

an output and signal-monitoring circuit having a function of applying the data signal to the data signal line

and a function of obtaining, as monitored data, data according to a magnitude of a signal flowing through the data signal line, the monitored data being base data for the characteristic data; and

an AD conversion circuit configured to convert the monitored data from an analog value to a digital value,

the output and signal-monitoring circuit includes:

an internal data line connected to the data signal line;

an operational amplifier having a non-inverting input terminal to which the data signal is provided, and an inverting input terminal connected to the internal data line;

a second capacitor having one end connected to the internal data line, and an other end connected to an output terminal of the operational amplifier;

a first control switch having one end connected to the internal data line, and an other end connected to the output terminal of the operational amplifier; and

a second control switch having one end connected to the data signal line, and an other end connected to the internal data line,

the AD conversion circuit is provided per plurality of the output and current-monitoring circuits,

when a row for which the characteristic detection process is performed during a frame period is defined as a monitored row, and a row other than the monitored row is defined as a non-monitored row, the frame period includes a characteristic detection processing period including a signal measurement period during which a characteristic of the characteristic detection target circuit element is detected by measuring a signal flowing through the data signal line,

the signal measurement period includes an AD conversion period during which the AD conversion circuit converts the monitored data from the analog value to the digital value, and

during the AD conversion period,

the data signal line and the internal data line are electrically disconnected from each other by bringing the second control switch into an off state, and

the AD conversion circuit sequentially converts the monitored data from analog values to digital values, the monitored data being obtained by corresponding output and signal-monitoring circuits.

16. The display device according to claim **15**, wherein the signal measurement period includes: a drive transistor characteristic detection period during which signal measurement for detecting a characteristic of the drive transistor is performed; and an electrooptical element characteristic detection period during which signal measurement for detecting a characteristic of the electrooptical element is performed.

17. The display device according to claim **16**, wherein

the signal measurement period further includes a data signal line charging period during which the data signal line is charged such that a signal of a magnitude according to the characteristic of the characteristic detection target circuit element flows through the data signal line,

the output and signal-monitoring circuit further includes a third control switch having one end connected to the data signal line, and an other end connected to a predetermined control line, and

in the drive transistor characteristic detection period included in the signal measurement period, during the AD conversion period, the data signal line and the control line are electrically connected to each other by bringing the third control switch into an on state, and a potential of a magnitude is provided to the control line, the magnitude being equal to a magnitude of a potential provided to the data signal line during the data signal line charging period.

18. The display device according to claim **17**, wherein in the electrooptical element characteristic detection period included in the signal measurement period, during the AD conversion period, the third control switch is brought into an off state and the monitoring control transistor is brought into an off state, so that the data signal line goes into a high-impedance state.

19. The display device according to claim **17**, wherein in the electrooptical element characteristic detection period included in the signal measurement period, during the AD conversion period, the data signal line and the control line are electrically connected to each other by bringing the third control switch into an on state, and a potential of a magnitude is provided to the control line, the magnitude being substantially equal to a magnitude of a potential provided to the data signal line during the data signal line charging period.

20. The display device according to claim **17**, wherein in the electrooptical element characteristic detection period included in the signal measurement period, during the AD conversion period, the data signal line and the control line are electrically connected to each other by bringing the third control switch into an on state, and a potential of certain magnitude is provided to the control line, the potential of certain magnitude being close to a potential to be provided to the data signal line during the data signal line charging period.

21. The display device according to claim **16**, wherein

the characteristic detection processing period further includes a detection preparation period during which preparation for detecting a characteristic of the characteristic detection target circuit element is performed in the monitored row,

when a potential provided to the data signal line during the detection preparation period is Vmg, a potential provided to the data signal line during the drive transistor characteristic detection period is Vm_TFT, and a potential provided to the data signal line during the electrooptical element characteristic detection period is Vm_oled, values of Vmg, Vm_TFT, and Vm_oled are set so as to satisfy following relationships:

$Vm\_TFT<Vmg-Vth(T2)$

$Vm\_TFT<ELVSS+Vth(oled)$

Vm_oled **22** Vmg−Vth(T**2**)

$Vm\_oled>ELVSS+Vth(oled)$

where Vth(T**2**) is a threshold voltage of the drive transistor, Vth(oled) is a light emission threshold voltage of the electrooptical element, and ELVSS is a cathode potential of the electrooptical element.

22. The display device according to claim **15**, wherein the characteristic detection processing period is provided in a vertical retrace period.

23. The display device according to claim **22**, wherein with any electrooptical element defined as a focused electrooptical element, when the focused electrooptical element

is included in the monitored row, the pixel circuit driving unit provides to the data signal line a potential of a data signal corresponding to a larger grayscale voltage than a grayscale voltage provided when the focused electrooptical element is included in the non-monitored row, upon performing writing of the data signal to a pixel circuit included in the monitored row during a vertical scanning period.

24. The display device according to claim **15**, wherein the characteristic detection processing period is provided in a vertical scanning period.

25. The display device according to claim **15**, wherein the characteristic detection process for only either one of the electrooptical element and the drive transistor is performed per frame period.

26. The display device according to claim **15**, wherein the output and signal-monitoring circuit has a function of obtaining, as the monitored data, data according to a magnitude of a current flowing through the data signal line.

27. The display device according to claim **15**, wherein the AD conversion circuit is provided per plurality of the output and signal-monitoring circuits.

28. The display device according to claim **15**, wherein the characteristic detection processing period further includes: a detection preparation period during which preparation for detecting a characteristic of the characteristic detection target circuit element is performed in the monitored row; and a light emission preparation period during which preparation for allowing the electrooptical element to emit light is performed in the monitored row.

29. The display device according to claim **15**, wherein the signal measurement period further includes: a data signal line charging period during which the data signal line is charged such that a signal of a magnitude according to the characteristic of the characteristic detection target circuit element flows through the data signal line; and a monitoring period during which the monitored data is obtained by accumulating a time-integrated value of the signal flowing through the data signal line in the second capacitor.

30. The display device according to claim **29**, wherein a cycle is repeated a plurality of times during a signal measurement period for detecting a characteristic of one characteristic detection target circuit element, the cycle including the data signal line charging period, the monitoring period, and the AD conversion period.

31. The display device according to claim **15**, wherein the characteristic detection processing period is provided immediately after the power is turned on or during a power-off period.

32. A method for driving a display device including: a pixel matrix of n rows×m columns including n×m pixel circuits (n and m are integers greater than or equal to **2**), each pixel circuit including an electrooptical element whose luminance is controlled by a current and a drive transistor for controlling a current to be supplied to the electrooptical element; scanning lines provided for the respective rows of the pixel matrix; monitoring control lines provided for the respective rows of the pixel matrix; data signal lines provided for the respective columns of the pixel matrix; and a pixel circuit driving unit configured to drive the scanning lines, the monitoring control lines, and the data signal lines, the method comprising:

a characteristic detecting step of detecting, during a frame period, a characteristic of a characteristic detection target circuit element including at least one of the electrooptical element and the drive transistor;

a correction data storing step of allowing a correction data storage unit to store characteristic data obtained based on results of the detection in the characteristic detecting step, as correction data for correcting video signals, the correction data storage unit being prepared in advance; and

a video signal correcting step of generating data signals to be supplied to the n×m pixel circuits by correcting the video signals based on the correction data stored in the correction data storage unit, wherein

each of the pixel circuits includes:

the electrooptical element;

an input transistor having a control terminal connected to the scanning line, a first conduction terminal connected to a control terminal of the drive transistor, and a second conduction terminal connected to the data signal line;

the drive transistor having a first conduction terminal to which a drive power supply potential is provided;

a monitoring control transistor having a control terminal connected to the monitoring control line, a first conduction terminal connected to a second conduction terminal of the drive transistor and an anode of the electrooptical element, and a second conduction terminal connected to the data signal line; and

a first capacitor having one end connected to the control terminal of the drive transistor to hold a potential of the control terminal of the drive transistor,

the pixel circuit driving unit includes:

an output and signal-monitoring circuit having a function of applying the data signal to the data signal line and a function of obtaining, as monitored data, data according to a magnitude of a signal flowing through the data signal line, the monitored data being base data for the characteristic data; and

an AD conversion circuit configured to convert the monitored data from an analog value to a digital value,

the output and current-monitoring circuit includes:

an internal data line connected to the data signal line;

an operational amplifier having a non-inverting input terminal to which the data signal is provided, and an inverting input terminal connected to the internal data line;

a second capacitor having one end connected to the internal data line, and an other end connected to an output terminal of the operational amplifier;

a first control switch having one end connected to the internal data line, and an other end connected to the output terminal of the operational amplifier; and

a second control switch having one end connected to the data signal line, and an other end connected to the internal data line,

the AD conversion circuit is provided per plurality of the output and signal-monitoring circuits,

when a row for which the characteristic detection process is performed during a frame period is defined as a monitored row, and a row other than the monitored row is defined as a non-monitored row,

the characteristic detecting step includes:

a detection preparing step of preparing for detecting a characteristic of the characteristic detection target circuit element in the monitored row;

a signal measuring step of detecting a characteristic of the characteristic detection target circuit element by measuring a signal flowing through the data signal line; and

a light emission preparing step of preparing for allowing the electrooptical element to emit light in the monitored row,

the signal measuring step includes:

a data signal line charging step of charging the data signal line such that a signal of a magnitude according to the characteristic of the characteristic detection target circuit element flows through the data signal line;

a monitoring step of obtaining monitored data by accumulating a time-integrated value of the signal flowing through the data signal line in the second capacitor; and

an AD converting step of converting, by the AD conversion circuit, the monitored data from the analog value to the digital value, and

in the AD converting step,

the data signal line and the internal data line are electrically disconnected from each other by bringing the second control switch into an off state, and

the AD conversion circuit sequentially converts the plurality of pieces of monitored data from analog values to digital values, the plurality of pieces of monitored data being obtained by a plurality of corresponding output and signal-monitoring circuits.

33. The method according to claim **32**, wherein the output and signal-monitoring circuit has a function of obtaining, as the monitored data, data according to a magnitude of a current flowing through the data signal line.

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专利名称(译)	显示装置及其驱动方法		
公开(公告)号	US20160300534A1	公开(公告)日	2016-10-13
申请号	US15/037712	申请日	2014-08-20
[标]申请(专利权)人(译)	夏普株式会社		
申请(专利权)人(译)	夏普株式会社		
当前申请(专利权)人(译)	夏普株式会社		
[标]发明人	KISHI NORITAKA		
发明人	KISHI, NORITAKA		
IPC分类号	G09G3/3283 G09G3/325		
CPC分类号	G09G3/3283 G09G3/325 G09G2330/028 G09G2300/0426 G09G2320/0295 G09G2320/046 G09G2300/0819 G09G2300/0842 G09G2320/0633 G09G3/3233 G09G2310/0262 G09G2320/043 G09G2320/045		
优先权	2013264466 2013-12-20 JP		
其他公开文献	US9842545		
外部链接	Espacenet USPTO		

摘要(译)

实现了能够在抑制电路尺寸增加的同时补偿电路元件劣化的显示装置。数据信号线（S（j））不仅用作传输信号的信号线，该信号允许每个像素电路（ 11 ）中的有机EL元件（OLED）发光。期望的亮度，但也用作特征检测的信号线。另外，在数据信号线（S（j））和内部数据线（Sin（j））之间提供开关（ 334 ）。在这样的配置中，在将用于特征检测的模拟数据转换为数字数据的AD转换时段期间，开关（ 334 ）进入关闭状态和数据信号线的电位。紧接在AD转换时段之前获得的（S（j））通过预定控制线（CL）提供给数据信号线（S（j））。